Computer architectures

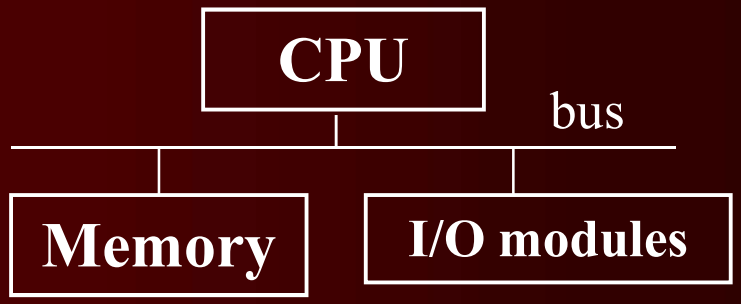
The processor

Általános
INFORMATIKAI
Tanszék

Today's program

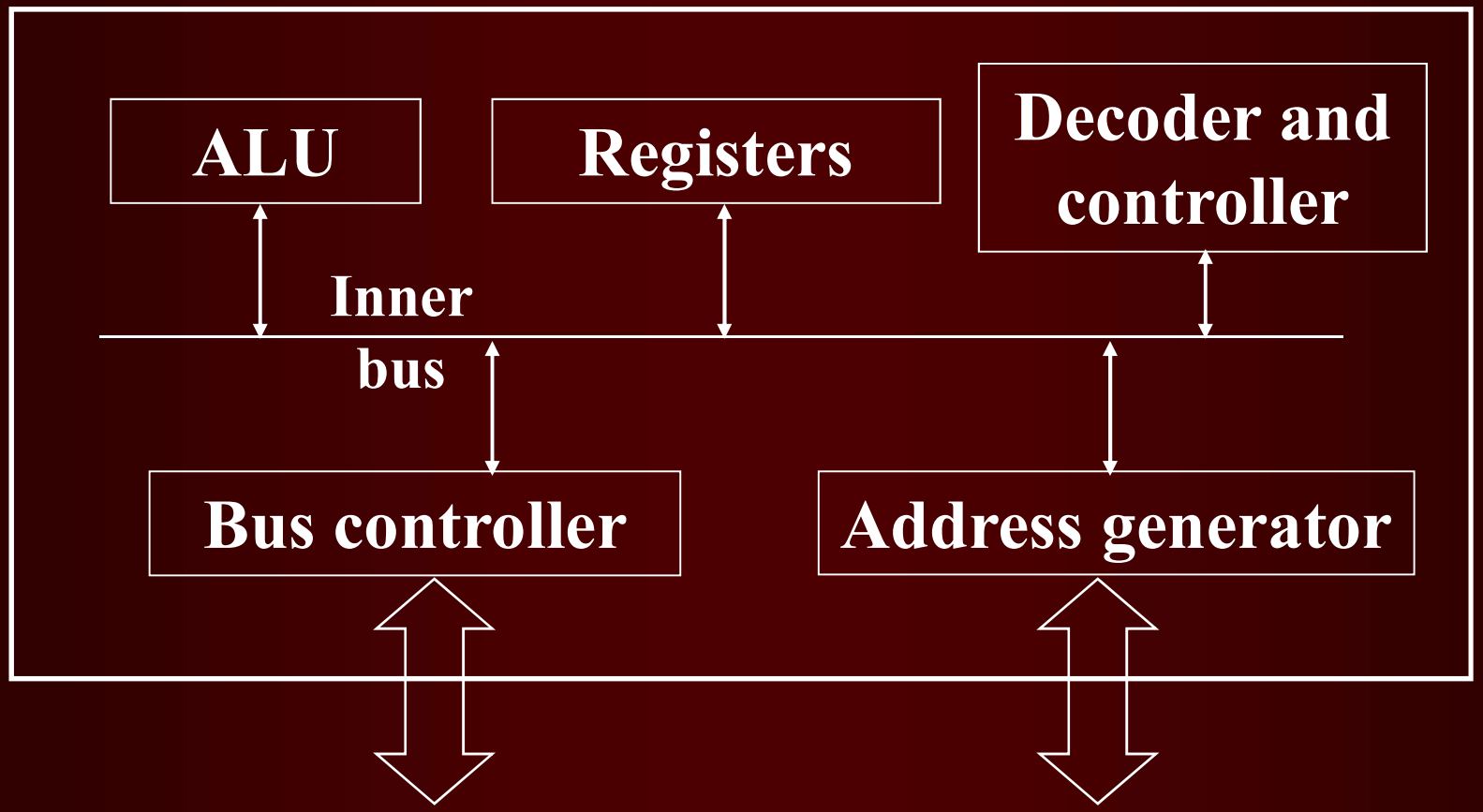
- The CPU and its parts
  - ALU, registers, controller, bus, MMU.
  - instruction set,
  - CPU runing modes.
- Performance measurement.

The Neumann architecture



- The main components
  - The CPU: central processing unit
  - The operational memory
  - Peripherals, devices, I/O modules
  - The bus
- The operation in general:
  - The CPU fetches the next machine instruction, analyzes and executes it. If necessary, it also fetches its data.
  - Some instructions can handle peripherals.

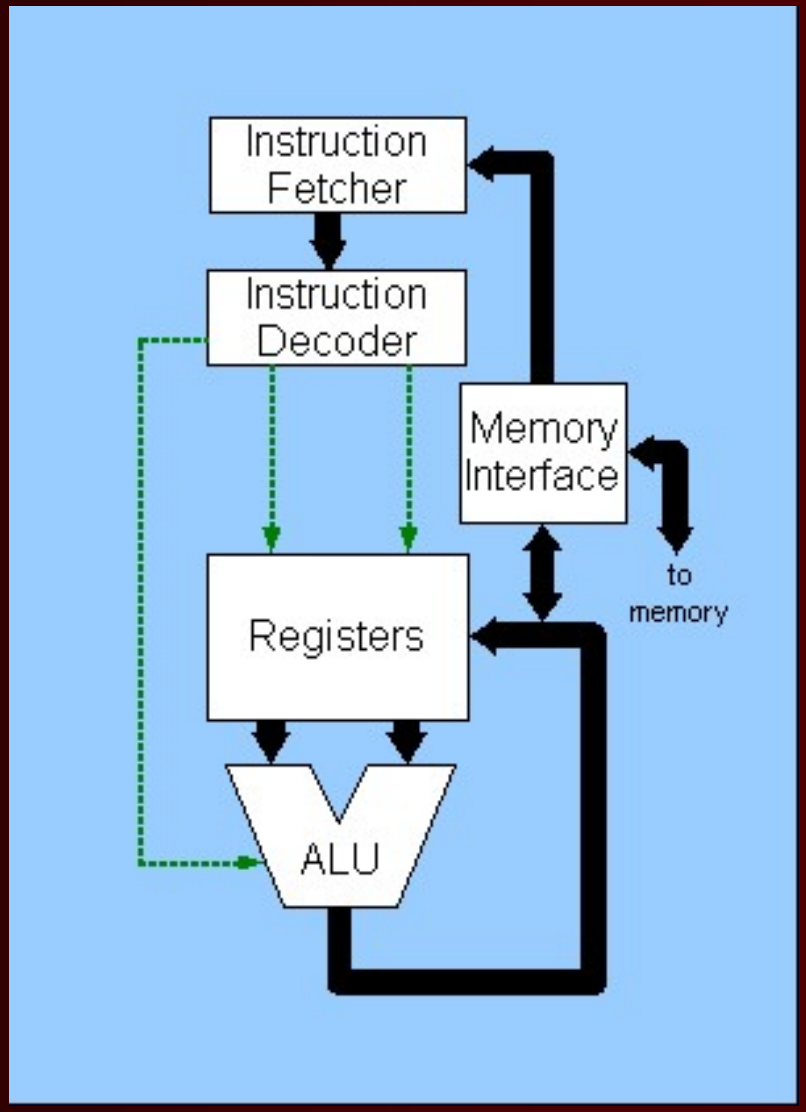
An imaginary CPU



Main parts of the CPU

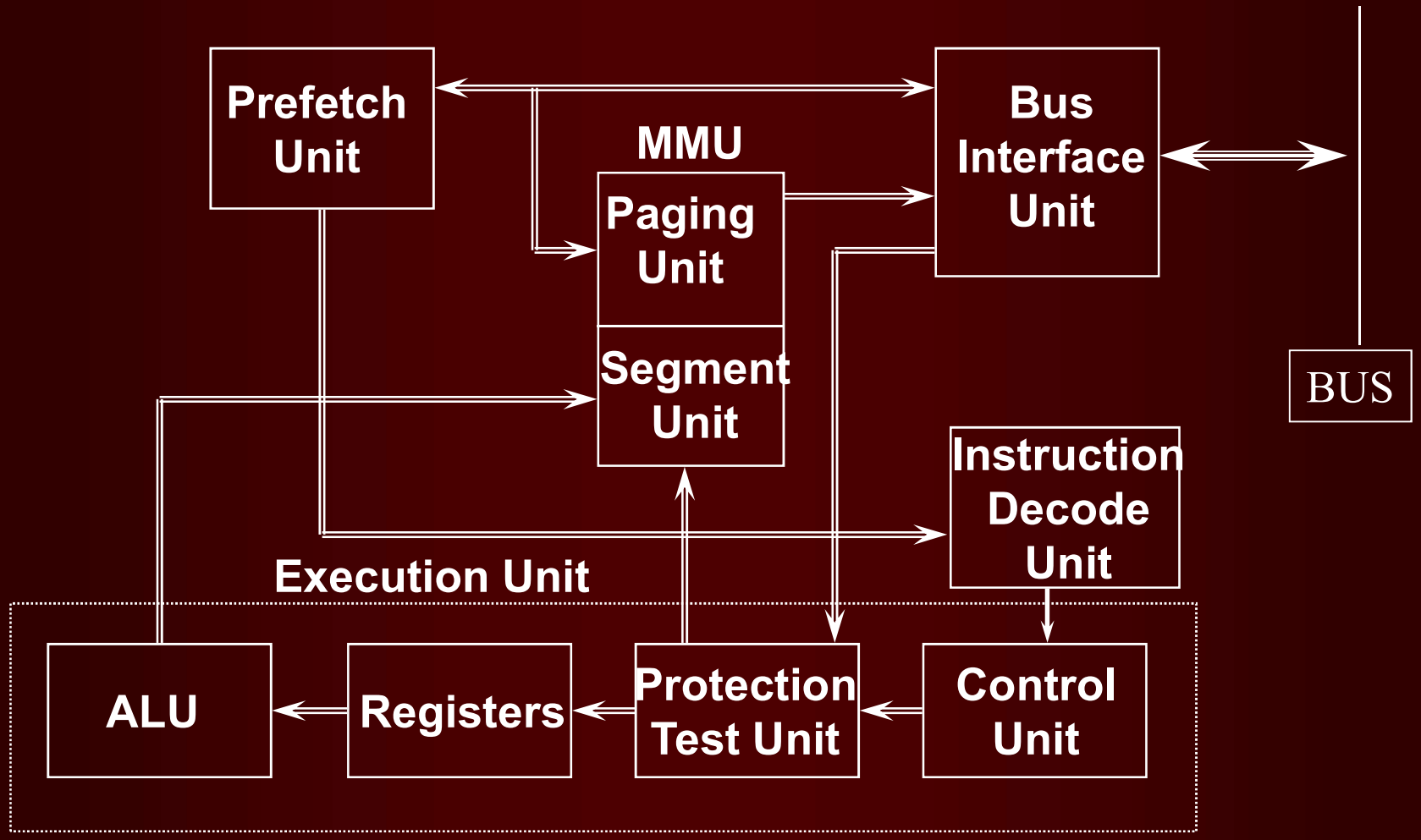
- In general, the main parts are:
  - the ALU (the calculator) also known as the execution unit (EU)
  - the register set (top of the storage hierarchy),
  - the decoder-control unit,
  - the bus driver,
    - address generator, protection unit,
    - the bus control unit .
- It can be more complicated,
  e.g. there can be several ALUs, etc.

CPU block diagram

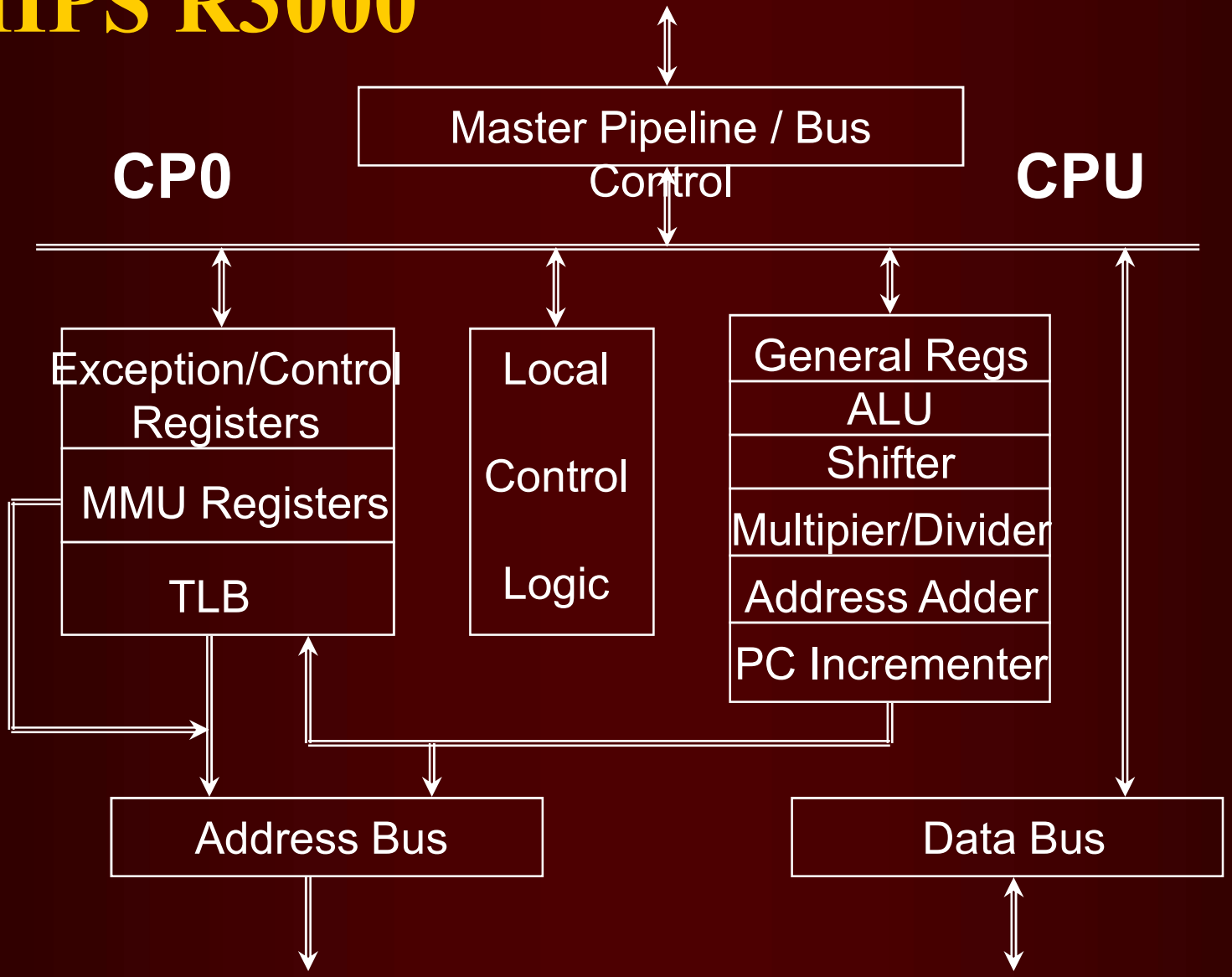


- **http://en.wikipedia.org/wiki/central_processing_unit**

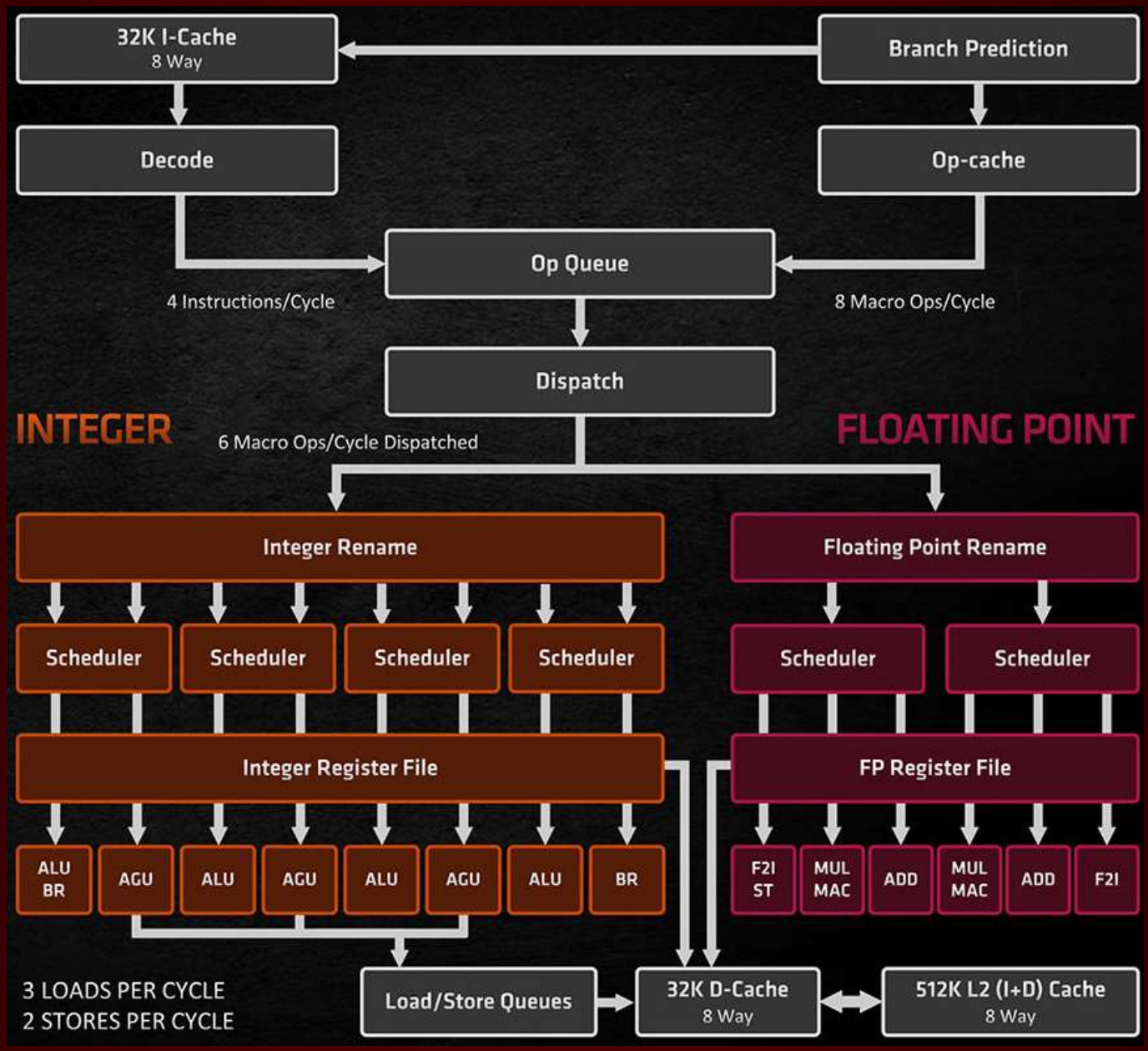
Intel 386


Prefetch Unit
MMU
Paging Unit
Segment Unit
Bus Interface Unit
BUS
Instruction Decode Unit
Execution Unit
ALU
Registers
Protection Test Unit
Control Unit

MIPS R3000


Master Pipeline / Bus Control
CP0
CPU
Exception/Control Registers
MMU Registers
TLB
Local Control Logic
General Regs
ALU
Shifter
Multipier/Divider
Address Adder
PC Incrementer
Address Bus
Data Bus

AMD “Zen 3” Microarchitecture



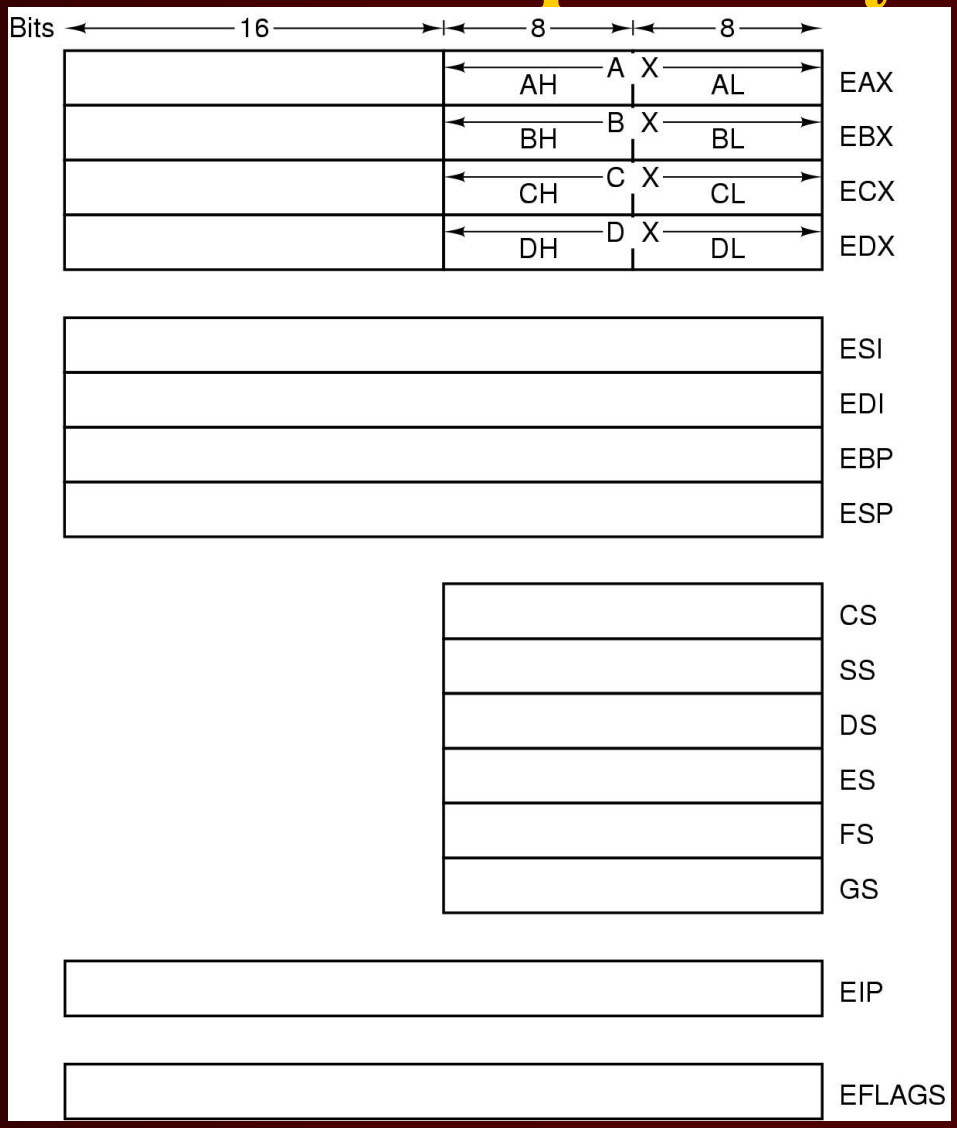
The ALU

- **Arithmetic and logical unit**
- **It can perform some (basic) operations:**
  - **addition, subtraction,**
  - **fixed-point multiplication, division,**
  - **Shifting (rotation),**
  - **comparisons (logical operations).**
- **We will look the instructions later...**
- **Floating point arithmetic?**
  - **Sometimes a separate processor for this.**

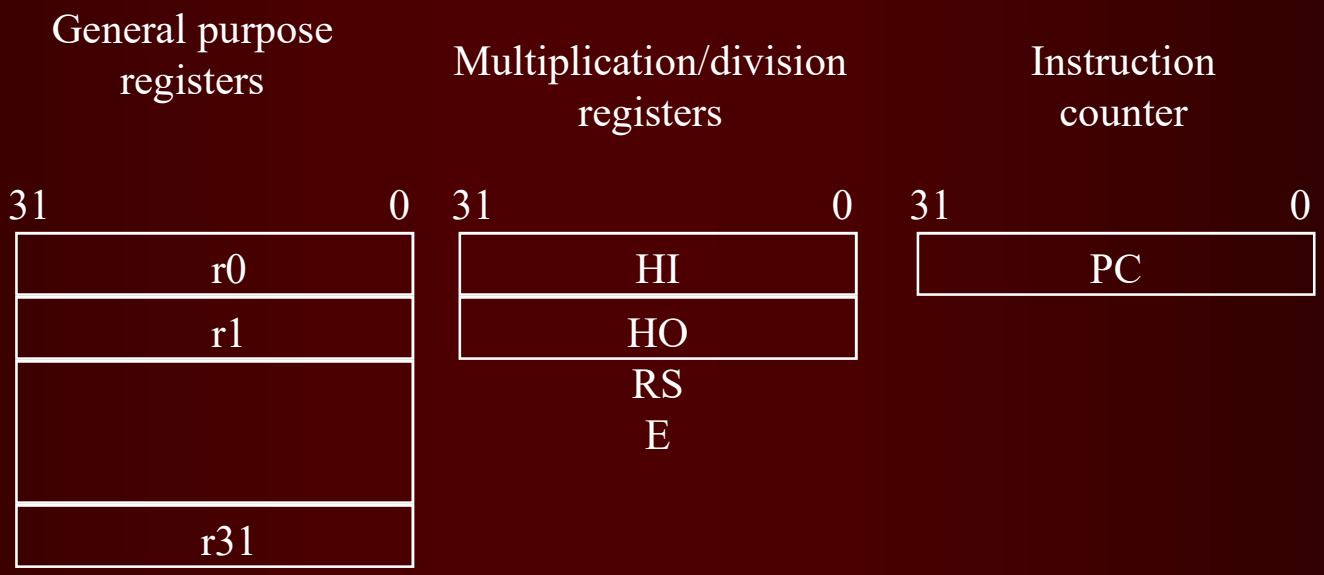
The registers

- **Internal storage of the CPU. Fastest access.**
  - **They provide working memory for the CPU,**
  - **help with address calculation,**
  - **they help control (e.g. by storing status parameters).**
- **Several of them have names (can be used by the programmer).**
- **They have different lengths (bit width),**
- **may be they are overlapping.**

Pentium II primary registers



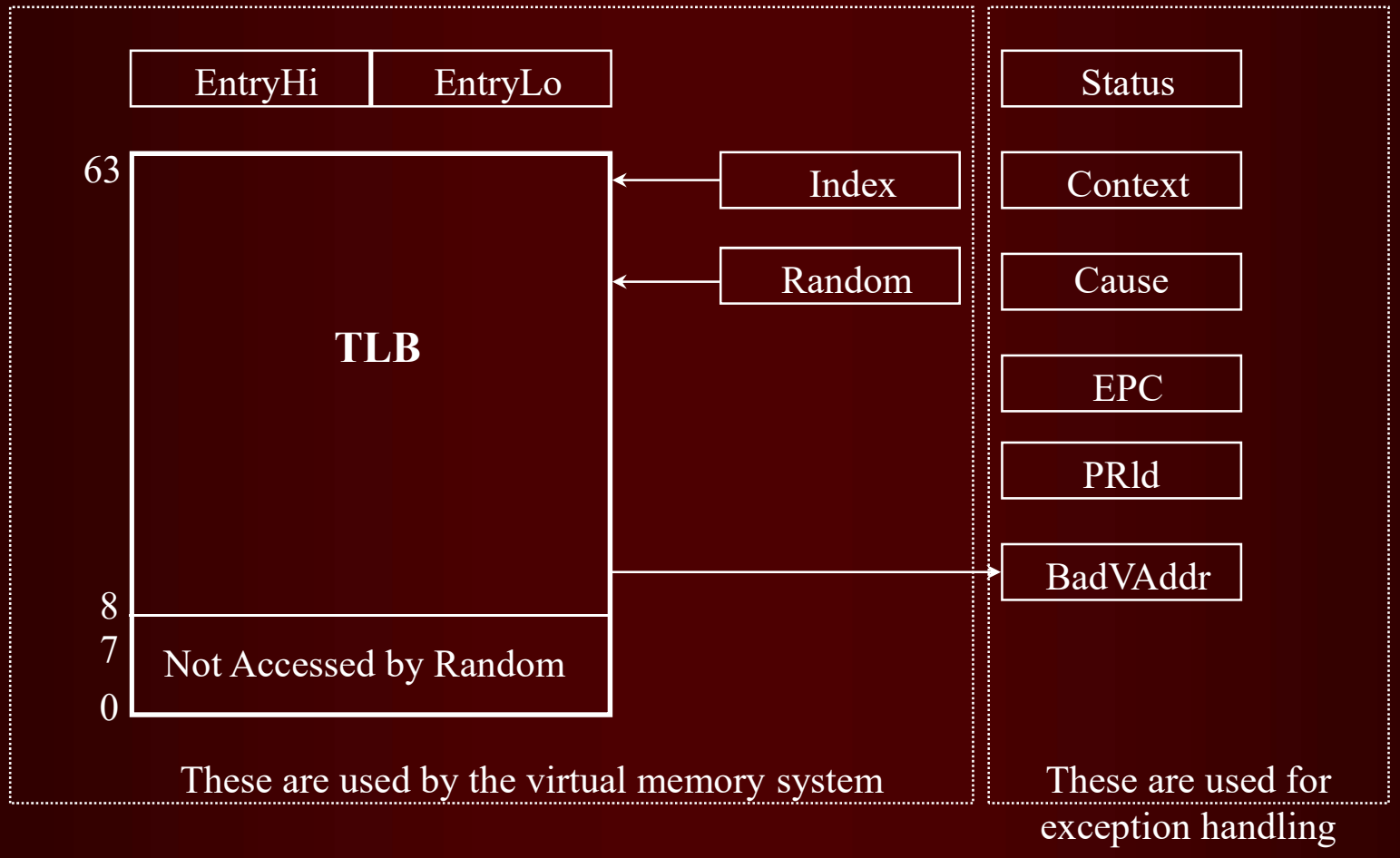
The registers of the R3000



Of these:

r0: contains hard-wired 0
r31: link register for jump-and-link instruction

SYSTEM COPROCESSOR REGISTERS



Classes of registers

- According to the (programming) use
  - **Visible** to programmers (user visible): applications and operating system programs can also use them.
    Within this, according to the way of use
    - **general** (can be used in any instruction),
    - **special** (can only be used in certain instructions).
  - **Limited use**: can be used by the processor, possibly the operating system core

Classes of registers

- According to the goal of the application
  - Data registers,
  - address registers,
    - Stack Pointer Register (SP) (shows the top of the stack)
    - Index register (base address + index gives the address),
    - Segment register (segment address and offset give address)
    - Register(s) pointing to address mapping table(s)
  - Control (special purpose) registers
    - Program counter register (PC: Program Counter; IP: Instruction Pointer)
    - Instruction Storage Register (IR)
    - Status register (PSW: Program Status Word)

Status register (PSW: Program Status Word)

- The status register summarizes the status bits reflecting the internal state of the CPU:
  - condition bits or flags (carry, zero, sign, overflow, etc.), which are set at the end of the instruction execution.
  - Mode bits (user/kernel mode) and the
  - IT mask (IT enable/disable).
- PSW and PC (Program Counter) together form the PSLW (Program Status Longword). It contains all important information about the status of the processor and the instruction stream.

PSW (8088):

0 carry, overflow, transmission
1 Reserved for development
2 parity
3 Subject to development
4 auxiliary carry, arithmetic overflow
5 Subject to development
6 zero, result is zero
7 signum, omen
8 traps, step-by-step execution
9 IT disabled, enabled
11 overflow
12-15 Reserved for development

The control and decoding unit

- Parse the **fetched machine instruction**,
- **decodes** (e.g. determines which microcodes will be used), and
- **controls other units of the CPU** (e.g. issues instructions).

The Bus of the CPU

- Circuits supporting the data traffic within the **CPU.**

The addressing and bus control unit

- the address generation and protection unit is helping to map real (physical) addresses from the logical (virtual) addresses
  - The TLB (Translation Lookaside buffer) (fixed number of slots, to map virtual addresses onto physical addresses)
  - The MMU supporting the segment management and paging
  - It may have a special protection subunit
- the bus controller is to fetch instructions from memory, get data from memory (load), move data to memory (store), get data from I/O modules (in) and move data to I/O modules (out).

The caches

- Cache memory in modern architectures
  - **Instruction cache** (I-Cache)
  - **Data cache** (D-Cache)
- Loads and stores **are done from the cache**, but this fact is sometimes ignored during the discussion
- Caches will be discussed later

Instruction Set Architecture (ISA)

- http://en.wikipedia.org/wiki/Instruction_set_architecture
- **The IA-32 architecture:**
  - http://en.wikipedia.org/wiki/IA-32
- ISA **describes the aspects of a computer architecture visible to a programmer**, including the native datatypes, instructions, registers, addressing modes, memory architecture, interrupt and exception handling, and external I/O (if any).
- An ISA is a specification of the set of all binary codes (opcodes) that are the native form of commands implemented by a particular CPU design. The set of opcodes for a particular ISA is also known as the **machine language** for the ISA.
- "Instruction set architecture" is sometimes used to distinguish this set of characteristics from the microarchitecture , which is the set of processor design techniques used to implement the instruction set (including microcode, pipelining, cache systems, and so forth). Computers with different microarchitectures can share a common instruction set . For example, the Intel Pentium and the AMD Athlon implement nearly identical versions of the x86 instruction set, but have radically different internal designs.

An imaginary microprocessor

- It has A, B, C, Test and IP registers
- The list on the right lists the instruction set
- 0 – 127 addresses are the PROM
- 128 - ... Addresses are the RAM
- The program below:

```
a=1; f=1;
while (a <= 5) {
f = f * a;
a = a + 1;
}
```

- LOAD reg,mem //reg ← (mem)
- CON reg,const //reg ← const
- SAVE reg,mem //mem ← (reg)
- ADD r1,r2,r3 //r1 ← (r2) + (r3)
- MUL r1,r2,r3 //r1 ← (r2) * (r3)
- COMP r1,r2 //T ← (r1) > (r2)
- JUMP mem //IP ← mem
- JG mem //if T, then IP ← mem
- STOP //Stop execution
- etc.

Mnemonics: a technique and science that helps memory and recall

Our program...

```
// Assume a is at address 128
// Assume f is at address 129
0 CON A,1 // a=1;
1 SAVE A,128
2 CON B,1 // f=1;
3 SAVE B,129
4 LOAD A,128 // if a > 5
5 CON B,5
6 COMP A,B
7 JG 17
8 LOAD B,129 // f=f*a;
9 LOAD A,128
10 MUL C,A,B
11 SAVE C,129
12 LOAD A,128        // a=a+1;
13 CON B,1
14 ADD C,A,B
15 SAVE C,128
16 JUMP 4     // loop back to if
17 STOP
```

```
a=1; f=1;
while (a <= 5) {
f = f * a;
a = a + 1;
}
```

The instruction set

- The CPU architecture specifies the set of instructions
- An instruction:
- There are everal addressing methods
  - direct and indirect memory addressing,
  - direct register addressing,
  - indirect register addressing,
    - Normal and pre/post auto de/incremental addressing,
  - relative addressing,
  - direct addressing.

- Two-operand instruction types according to the operands
  - Register-to-register ("cheaper")
  - Register-to-memory ("more expensive")
  - Register-to-I /O
- Memory addresses are logical addresses. The MMU supports the physical address calculation.
- Orthogonal instruction set: all addressing modes exist for all instructions

Addressing modes

- **Direct memory addressing**
  ADDRESS → memory content → operand
- **Indirect memory addressing**
  ADDRESS → memory content → address of operand → operand
- **Direct register addressing**
  ADDRESS → register → operand
- **Indirect register addressing**
  ADDRESS → register → operand address → operand
  [++|--] SP register [++|--] → operand address → operand
- **Relative addressing**
  ADDRESS → register, offset → address of operand + offset → operand
- **Direct addressing**
  ADDRESS → operand

Instruction groups

- Arithmetic and logical instructions
  - ADD|SUB| MUL|DIV|
  - AND|OR|XOR|NOT|NEG|COMPL
  - BODY|COMPARE
- Bit shifting, rotations, incrementation, decrementation
  - SHIFT|SLL|SLR|SLA|SRA|RCL|RCR
  - ROL|ROR
  - INC|DEC

Additional instruction groups

- Data handling instructions
  - LOAD|STORE|LB|LW|SB|SW ...
  - MOVE
  - IN|OUT
- Stack handling instructions
  - PUSH|POP|PUSHALL|POPALL

More groups

- **Jumps, branches**
  - **Unconditional: JUMP|BRANCH**
  - **Conditional: J(condition): JZ|JS|JC ... BZ|BS|BC ...**

And more groups

- Cycle creation instructions
  - LOOP|REP
- Calls, returns, process switching

  CALL|RET|IT|IRET

  BREAK|WAIT|NOP

  PMTSW (Protected Mode Task Switch)
- Coprocessor instructions

  FINITE

  FLD|FST

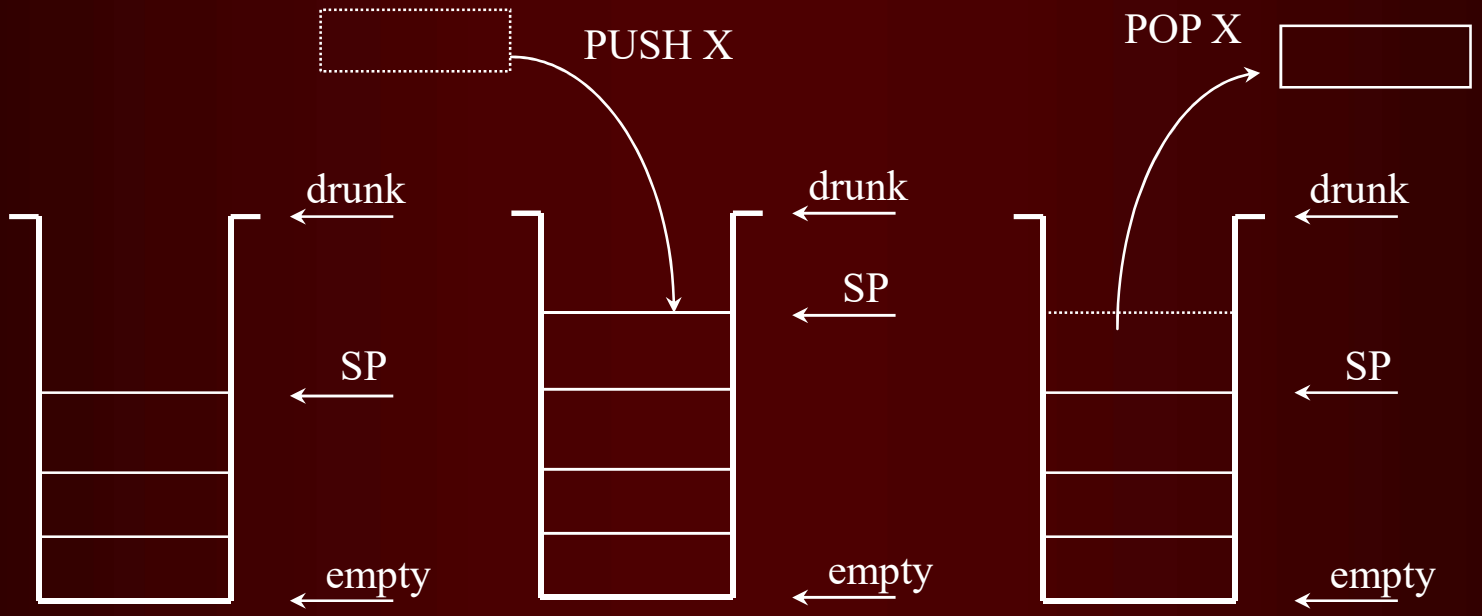
  FADD|FSUB|FMUL ...

  FWAIT

Stack, stack management instructions

- The stack is an abstract data structure, but
- nowdays processors are supporting them.
- It is implemented on the segments of the operational memory.
- MOVE instructions can also handle them: the abstract boundary conditions are violated.
- Let's look at the figure! See the effect of the PUSH/POP, and the change of SP!

Stack memory



The MMU

- Tasks of the Memoria Management Unit
  - Helps the logical-physical addressing,
    - address arithmetic in hardware,
    - in close cooperation with the OS.
    - sometimes using a TLB. (Translation Lookaside Buffer)
  - helps memory protection.
  - Cooperate with the bus controller.
- It is really only understandable in conjunction with OS memory management, so we postpone the topic ...
- Please note:
  memory access is done via caches ...

Operating modes of processors

- There are at least two ways (often more)
  - normal (user) mode ,
  - protected (kernel (supervisor, executive)) mode More privileged.
- In more privileged modes:
  - the instruction set is wider,
  - the address range is wider.
- The mode change: by the trap. OS controlled task.
- The current mode is always registered.

Famous processors

- Intel Pentium II, III, Celeron, Xeon, IV
- Itanium
- AMD Opteron, Turion, Athlon
- MIPS R3000,4000,5000,12000,14000
- DEC Alpha 21064, 21164, 21264A, 21364
- IBM RS64 II, Power2, Power3-II, Power4
- HP PA-RISC 8500, 8900
- SUN Sparc 20, SuperSPARC, UltraSPARC IV

Intel microprocessor history

Name	Date	Transistors	Microns	Clock speed	Data width (ALU)	MIPS
8080	1974	6,000	6	2 MHz	8 bits	0.64
8088	1979	29,000	3	5 MHz	16-bit 8-bit bus	0.33
80286	1982	134,000	1.5	6 MHz	16 bits	1
80386	1985	275,000	1.5	16 MHz	32 bits	5
80486	1989	1,200,000	1	25 MHz	32 bits	20
Pentium	1993	3,100,000	0.8	60 MHz	32-bit 64-bit bus	100
Pentium II	1997	7,500,000	0.35	233 MHz	32-bit 64-bit bus	~300
Pentium III	1999	9,500,000	0.25	450 MHz	32-bit 64-bit bus	~510
Pentium 4	2000	42,000,000	0.18	1.5 GHz	32-bit 64-bit bus	~1,700

Intel - Moore's Law

	Year	Number of transistors
4004	1971	2,250
8008	1972	2,500
8080	1974	5,000
8086	1978	29,000
286	1982	120,000
386™ processor	1985	275,000
486™ DX processor	1989	1,180,000
Pentium® processor	1993	3,100,000
Pentium II processor	1997	7,500,000
Pentium III processor	1999	24,000,000
Pentium 4 processor	2000	42,000,000

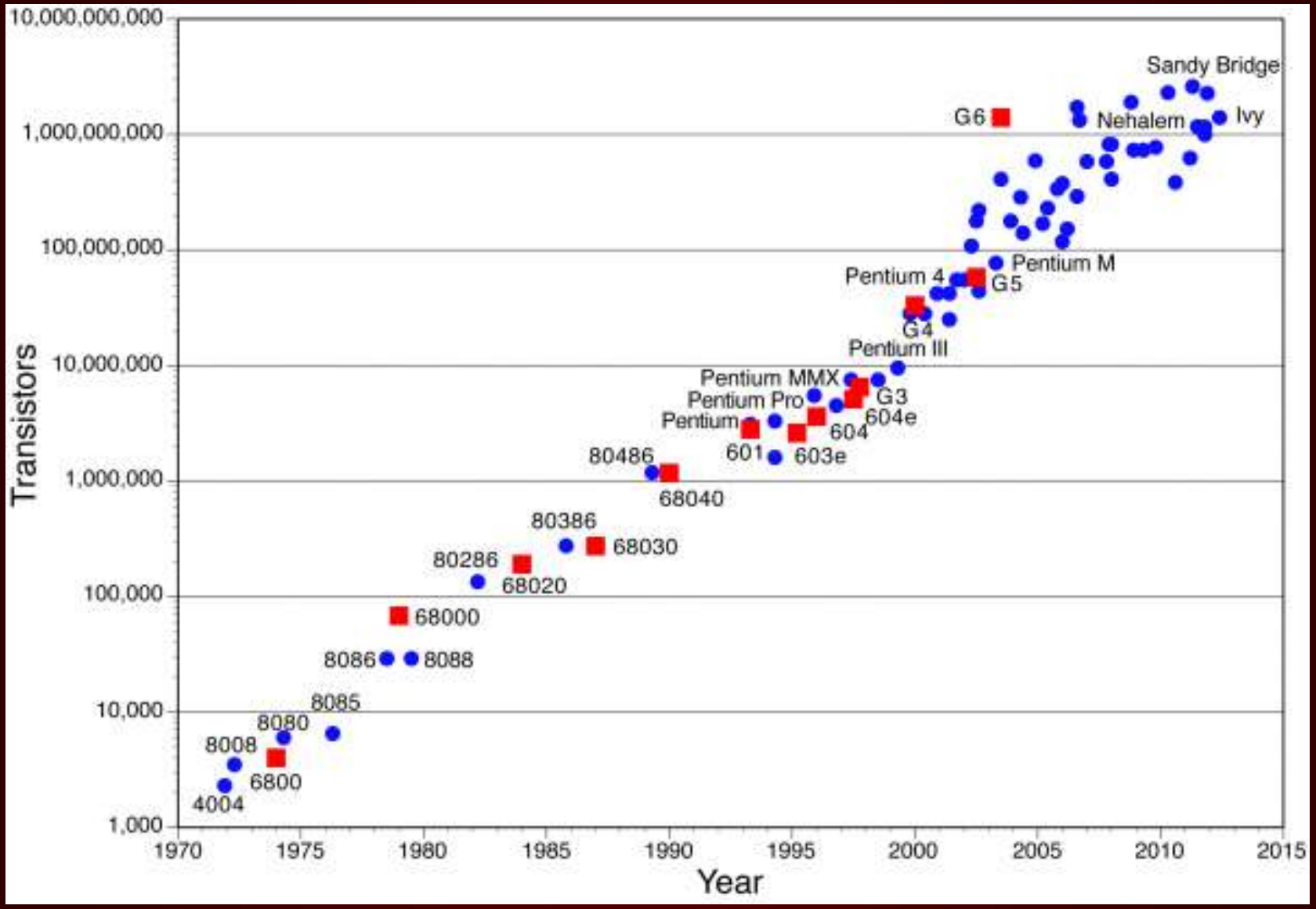
Z80, 1976, 8500

Gordon Moore :

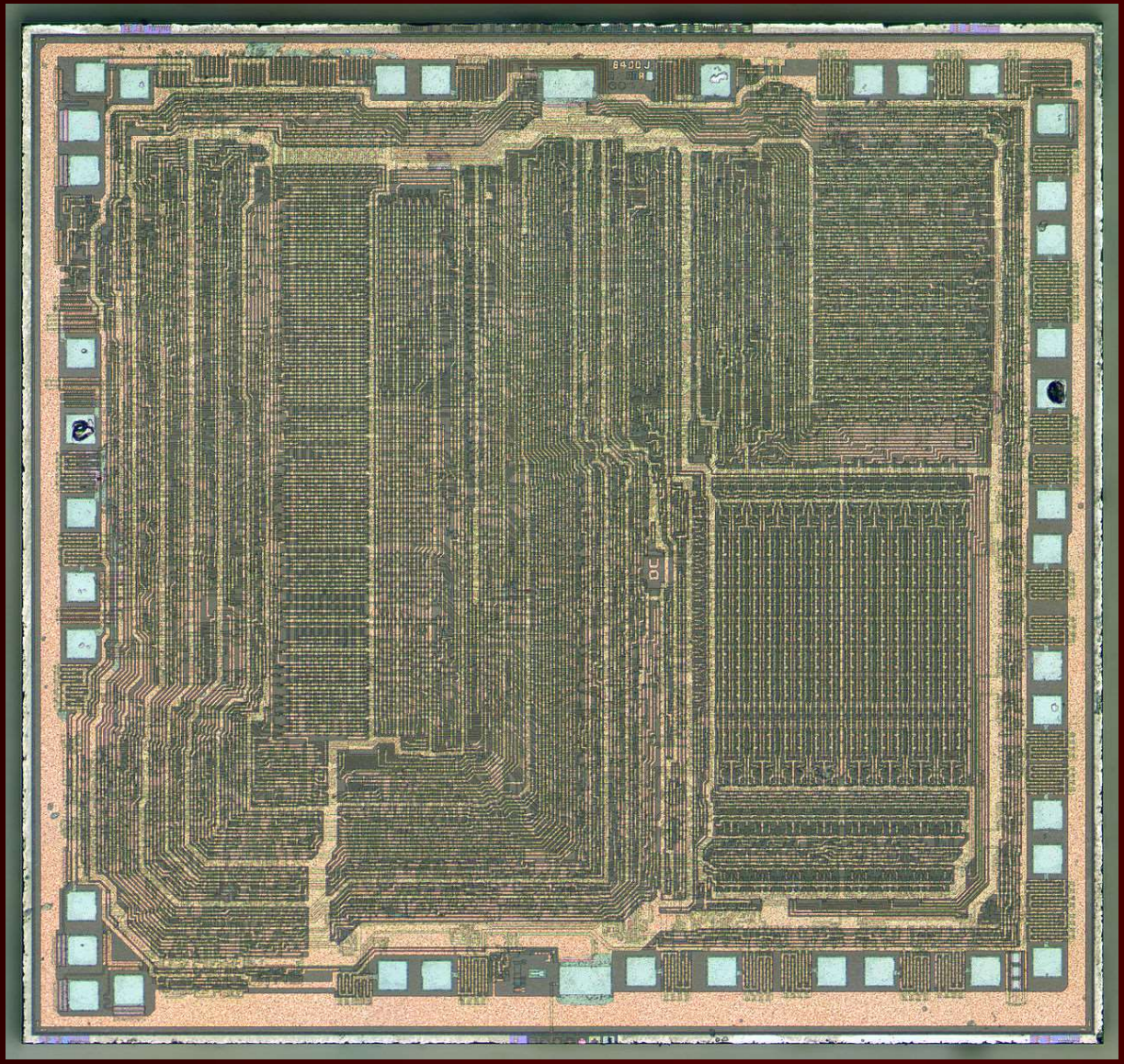
the number of the transistors in integrated circuits doubles every year (1965), every two years (1975).

1961 Discovery of the integrated circuit

Intel - Moore's Law

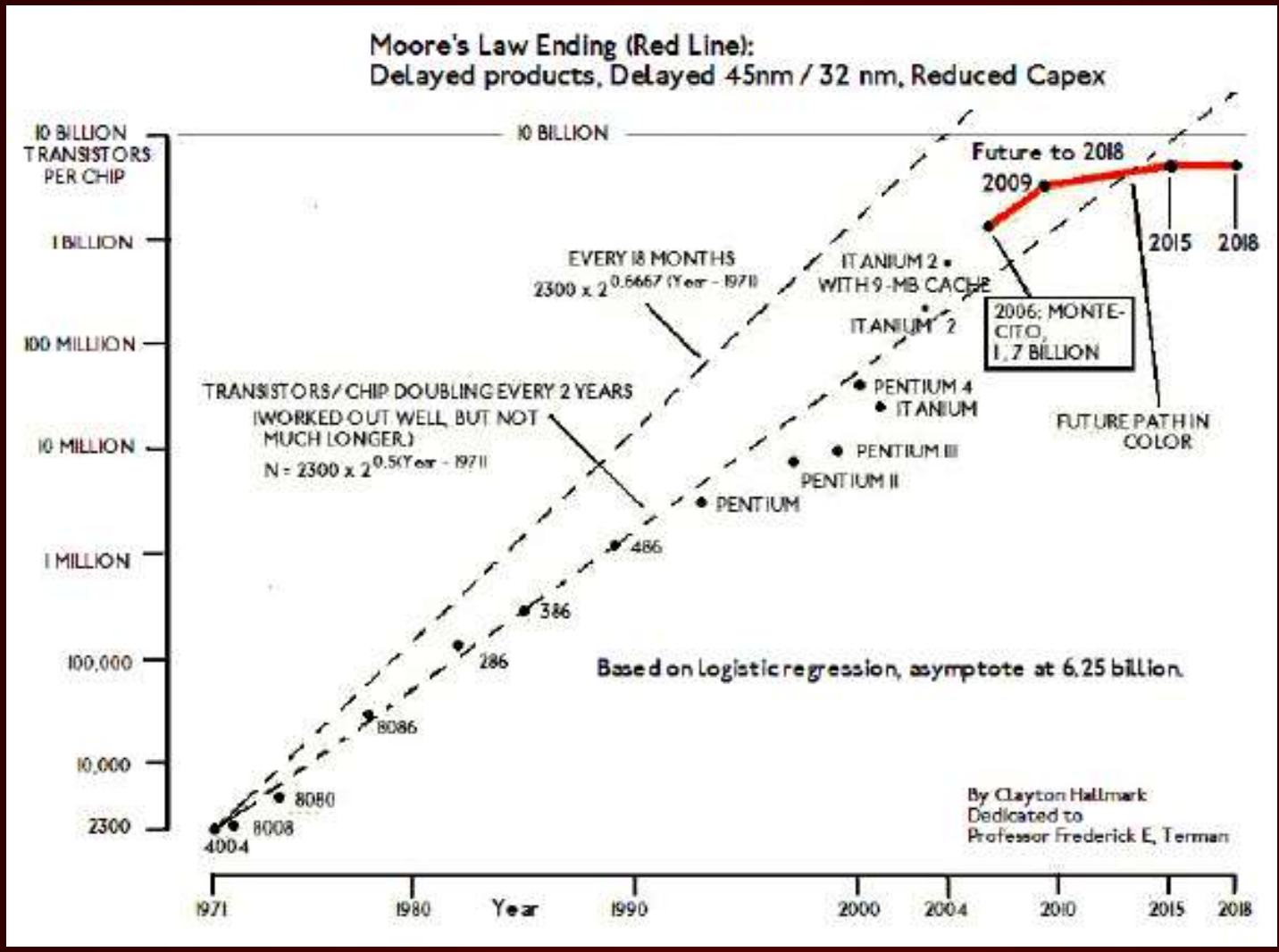


Intel - Moore's Law



Z80 , 1976,
8500 transistors,
4 µm ,
3545×3350 µm
recommended
until 2008,
still used today

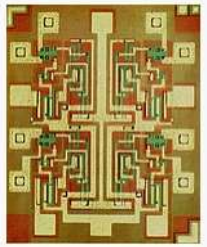
Intel - Moore's Law - End



https://www.indybay.org/newsitems/2006/05/18/18240941.php

https://en.wikipedia.org/wiki/Moore's_law

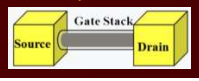
Semiconductor device fabrication



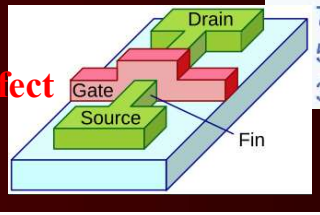
MOSFET scaling (process nodes)

- 20 µm – 1968
- 10 µm – 1971
- 6 µm – 1974
- 3 µm – 1977
- 1.5 µm – 1981
- 1 µm – 1984
- 800 nm – 1987
- 600 nm – 1990
- 350 nm – 1993
- 250 nm – 1996
- 180 nm – 1999
- 130 nm – 2001
- 90 nm – 2003
- 65 nm – 2005
- 45 nm – 2007
- 32 nm – 2009
- 28 nm – 2010
- 22 nm – 2012
- 14 nm – 2014
- 10 nm – 2016
- 7 nm – 2018
- 5 nm – 2020
- 3 nm – 2022

2 nm RibbonFET



fin field-effect transistor FinFET



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Intel - Moore's Second Law

Moore's Second Law: About handy little commodity computers.

Arthur Rock or Gordon Moore: The cost of a semiconductor chip fabrication plant doubles every four years

Moore's article in which he stated his law really was about Commoditization of Computers. Super-cheap computers, $100 or so, can kill his company, Intel, Microsoft, and, especially, Dell Inc.

"What I need is a small-cheap computer to carry on my infinite-gas-mileage bicycle. Then I can just throw it away if I break it."

"In the future, computer performance will be sacrificed for portability and power savings ."

"We need cheaper, not better ."

Dell Inc., Intel, Microsoft -- all will go down with Moore's Law , by Kurt Kress
https://www.indybay.org/newsitems/2006/05/18/18240941.php

CPU performance measurement

- **CPU cycles. Why? The cycle time.**
- **It may take 1, 2, or a few hundred cycles to execute a machine instruction. IA** (Intel Architecture) **examples.**
- **Increasing the operating frequency reduces the cycle time. Where is the limit? Technology dependence.**

time-per-task = C * T * I

where:

C is the number of cycles per instruction,

T is the cycle time,

I is the number of instructions for the task.

The MIPS performance measurement

- **Million instructions per second: MIPS**

$$MIPS_i = 1/(T * C_i)$$

where i is the i-th instruction. But which one?

- Big differences in the number of cycles required!
- It's simple, though

we never write a program consisting only the i-th instructions.

- You can give a weighted average, but what should be the weighting?

The "standard" load classes

- **a given type of task** (integral arithmetic, floating-point arithmetic, graphic, transactional, etc.) **load programs** (**benchmark**), and
  - it is measured by running
  - and statistically weighted.
  - Different load classes and metrics
- Whetstone, Livermore Loops, Dhrystone, Linpack benchmarks.
- TPC Benchmark A (http://www.tpc.org)
- SPEC (http://www.spec.org)

SPEC: Standard Performance Evaluation Corporation

- It was founded in 1989. Nonprofit organization.
  - SPEC_ratio, VAX11-780 is the reference machine
- from 1992:
  - SPECint92: 8 normalized integer test geometric average.
  - SPECfp92: 14 normalized floating point tests geom. avg.
- from 1995 (reference: SPARCstation 10/40)
  - CINT95
  - CFP95
- from 2000
  - CINT2000 (12 tests, 4 metrics)
  - CFP2000 (14 tests, 4 metrics)

SPEC CPU 2006

- Comparison machine: Sun UltraSparc II., 296 MHz
- CINT2006 (12 tests, 4 metrics) fabric
  - SPECint2006
  - SPECint_base2006
  - SPECint_rate2006
  - SPECint_rate_base2006
- CFP2006 (14 tests, 4 metrics) fabric
  - SPECfp2006
  - SPECfp_base2006
  - SPECfp_rate2006
  - SPECfp_rate_base2006

SPEC CPU 2017

- The SPEC CPU 2017 benchmark package contains 43 benchmarks, organized into four suites:
  - The SPECspeed ® 2017 Integer and SPECspeed ® 2017 Floating Point suites are used for comparing time for a computer to complete single tasks.
  - The SPECrate ® 2017 Integer and SPECrate ® 2017 Floating Point suites measure the throughput or work per unit of time.
- SPEC CPU2017 focuses on compute intensive performance:
  - Processor - The CPU chip(s).
  - Memory - The memory hierarchy, caches and main memory.
  - Compilers - C, C++, and Fortran compilers, including optimizers.

The metrics

- "Speed" metrics (no "rate"): for comparing machines with one processor. (How long does the test take)
  - (unnamed, peak): with aggressive optimizing compilers
  - base: conservative translation
- "Throughput" metrics (rate) : for comparing multiprocessor machines. (The test is run in many instances, and the number of instances run in a unit of time is measured.)
  - (unnamed, peak): with aggressive optimizing compilers
  - base : conservative translation

SPEC Cloud IaaS 2016

- Benchmark suite to measure cloud performance
- Performance of infrastructure-as-a-service (IaaS) cloud platforms
- Cloud using I/O and CPU intensive cloud computing workloads:
  - social media
  - NoSQL database transaction
  - K-Means clustering using map/reduce as two significant and representative workload types within cloud computing
- Each workload runs in multiple instances
- The benchmark runs the workloads until quality of service (QoS) conditions are reached.

Software as a Service (**SaaS**),
Platform as a Service (**PaaS**),
Infrastructure as a Service (**IaaS**)

SPEC Cloud IaaS 2016

- **Scalability** measures the **total amount of work performed by application instances running in a cloud**. Application instances should scale linearly in an ideal cloud. Scalability is reported for the **number of compliant application instances** (AIs) **completed.**
- **Elasticity** measures **whether the work performed by application instances scales linearly in a cloud** when **compared to the** performance of application instances during **the baseline phase.** Elasticity **is expressed as a percentage.**
- **Mean Instance Provisioning Time** measures **the time interval between the instance provisioning request and connectivity** to port 22 on the instance. This metric is **an average across all instances** in valid application instances.

SPECint, SPECfp

- AI, go game
- Moto88K chip sim.
- CC version
- compressor-decompr.
- LISP interpreter
- jpeg graph compress-decompr
- AB operator
- finite element mesh generator
- rippling water model (1024*1024 grid)
- Monte Carlo simulation
- hydrodynamic equations
- 3D tense. field calculation
- partial diff. one. solution
- simulated turbulence calculation
- meteorological model
- quantum chemistry problem
- plasma physics problem

IDEAS Top Performers

- **IDEAS Top Performers - SPECint2000**
  http://www.ideasinternational.com/ (discontinued)
  - Benchmark menu item,
    - SPEC submenu item ...
- **TOP500 Supercomputers**
  http://www.top500.org/
- **Standard Performance Evaluation Corporation**
  Speed: [SPECint2006, SPECfp2006]
  Throughput: [SPECint_rate2006, SPECfp_rate2006]
  https://www.spec.org/cpu2006/results/

April 2000

IDEAS Top Performers - SPECint2000

Rank	Company	System	# CPU	Processor	Result	Baseline
1	Compaq Computer Corporation	AlphaServer DS20E Model 6/667	1	Alpha 21264A	444	424
2	Compaq Computer Corporation	AlphaServer ES40 Model 6/667	1	Alpha 21264A	433	413
3	Hewlett Packard Corporation	HP 9000 Model N4000	1	552 MHz PA-RISC 8500	379	367
4	SGI	SGI 2200 2X 400MHz R12k	2	R12000	347	334
5	Compaq Computer Corporation	AlphaServer DS20 Model 6/500	1	Alpha 21264	313	300
6	SGI	SGI 2200 2X 300MHz R12k	2	R12000	264	254
7	IBM Corporation	RS/6000 SP-375MHz T/W (1 CPU)	1	Power3-II	260	248
8	IBM Corporation	RS/6000 44P-270 (1 CPU)	1	Power3-II	251	242
9	IBM Corporation	RS/6000 44P-170 (400 MHz)	1	Power3-II	249	239
10	IBM Corporation	RS/6000 44P-170 (333 MHz)	1	Power3-II	180	177
11	Compaq Computer Corporation	AlphaServer 4100 5/533	1	Alpha 21164	--	176
12	Compaq Computer Corporation	AlphaStation 500/500	1	Alpha 21164	--	163
13	Fujitsu Siemens Computers	CELSIUS 650	1	Pentium III processor	--	337
14	Compaq Computer Corporation	DIGITAL Personal Workstation 500au	1	Alpha 21164	--	161
15	Intel Corporation	Intel OR840 motherboard	1	733 MHz Pentium III processor	--	336
16	Dell Computer Corporation	Precision WorkStation 410 (700 MHz, Pentium III processor)	1	Pentium III processor (700 MHz, 100 MHz bus)	--	307
17	Dell Computer Corporation	Precision WorkStation 420 (733 MHz, Pentium III processor)	1	Pentium III processor (733 MHz, 133 MHz bus)	--	336
18	IBM Corporation	RISC System/6000 H70 (1 CPU)	1	RS64 II	--	168
19	Sun Microsystems	Ultra 10 333MHz	1	UltraSPARC-IIi	--	133

March 2001

IDEAS Top Performers - SPECint2000

Rank	Company	System	# CPU	Processor	Result	Baseline
1	Compaq Computer Corporation	AlphaServer ES40 Model 6/833	1	Alpha 21264B	544	518
2	Intel Corporation	Intel D850GB motherboard(1.5 GHz, Pentium 4 processor)	1	Pentium 4 processor (1.5 GHz, 400 MHz bus)	536	524
3	Fujitsu Siemens Computers	CELSIUS 460	1	Pentium 4 processor (1.5 GHz, 400 MHz bus)	535	524
4	Alpha Processor, Inc.	API UP2000 833 MHz	1	Alpha 21264A	533	511
5	Dell	Precision WorkStation 330 (1.50 GHz P4)	1	Pentium 4	526	515
6	Intel Corporation	Intel D850GB motherboard(1.4 GHz, Pentium 4 processor)	1	Pentium 4 processor (1.4 GHz, 400 MHz bus)	512	502
7	Dell	Precision WorkStation 330 (1.40 GHz P4)	1	Pentium 4	505	493
8	Advanced Micro Devices	Gigabyte GA-7DX Motherboard 1.2GHz Athlon processor	1	1.2GHz AMD Athlon processor A1200AMT3C	496	443
9	Intel Corporation	Intel D850GB motherboard(1.3 GHz, Pentium 4 processor)	1	Pentium 4 processor (1.3 GHz, 400 MHz bus)	483	473
10	Sun Microsystems	Sun Blade 1000 Model 1900	1	UltraSPARC-III	467	438
11	Intel Corporation	Intel VC820(1.13 GHz Pentium III processor)	1	Pentium III processor (1.13 GHz, 133 MHz bus)	464	461
12	Dell	Precision WorkStation 420 (1.0 GHz PIII)	1	Pentium III	462	454
13	Advanced Micro Devices	ASUS A7V Motherboard 1.2GHz Athlon processor	1	1.2GHz AMD Athlon processor A1200AMT3B	458	409
14	Alpha Processor, Inc.	API UP2000 750 MHz	1	Alpha 21264A	456	434
15	Intel Corporation	Intel VC820 (1.0B GHz, Pentium III processor)	1	Pentium III processor (1.0B GHz, 133 MHz bus)	448	442
16	Compaq Computer Corporation	AlphaServer DS20E Model 6/667	1	Alpha 21264A	444	424
17	Intel Corporation	Intel OR840(1 GHz Pentium III processor)	1	Pentium III processor (1 GHz, 133 MHz bus)	442	438
18	Hewlett Packard Corporation	hp visualize j6000 UNIX workstation	1	552 MHz PA-8600	441	417
19	Dell	Precision WorkStation 420 (933 MHz PIII)	1	Pentium III	440	433
20	Compaq Computer Corporation	AlphaServer ES40 Model 6/667	1	Alpha 21264A	433	413

March 2002

IDEAS Top Performers - SPECint2000

RTHENK	Company	System	#CpU	Processor	Result	Baseline	Body Date
1	IBM Corporation	IBM eServer pSeries 690 Turbo	1	POWER4	814	790	Nov-01
2	Dell	Precision WorkStation 340 (2.2 GHz P4)	1	Intel Pentium 4	811	790	Jan-02
3	Dell	Precision WorkStation 530 (2.2 GHz Xeon)	1	Intel Xeon	810	788	Jan-02
4	Dell	Precision WorkStation 340 (2.2 GHz P4)	1	Intel Pentium 4	806	786	Jan-02
5	Dell	Precision WorkStation 530 (2.2 GHz Xeon)	1	Intel Xeon	802	784	Jan-02
6	Intel Corporation	Intel D850MD motherboard (2.2 GHz, Pentium 4 processor)	1	Pentium 4 processor (2.2 GHz, 400 MHz bus)	784	771	Nov-01
7	Dell	Precision WorkStation 340 (2.0A GHz P4)	1	Intel Pentium 4	759	738	Jan-02
8	Dell	Precision WorkStation 530 (2.0 GHz Xeon)	1	Intel Xeon	757	736	Jan-02
9	Dell	Precision WorkStation 340 (2.0A GHz P4)	1	Intel Pentium 4	753	735	Jan-02
10	Dell	Precision WorkStation 530 (2.0 GHz Xeon)	1	Intel Xeon	750	733	Jan-02
11	Intel Corporation	Intel D850MD motherboard (2.0A GHz, Pentium 4 processor)	1	Pentium 4 processor (2.0A GHz, 400 MHz bus)	735	722	Nov-01
12	Advanced Micro Devices	Epox 8KHA+ Motherboard, AMD Athlon (TM) XP 2000+	1	AMD Athlon(TM) XP 2000+	724	697	Jan-02
13	Advanced Micro Devices	Epox 8KHA+ Motherboard, AMD Athlon (TM) XP 1900+	1	AMD Athlon(TM) XP 1900+	701	677	Oct-01
14	Compaq Computer Corporation	AlphaServer ES45 Model 68/1000	1	Alpha 21264C	679	621	Jun-01
15	Advanced Micro Devices	Epox 8KHA+ Motherboard, AMD Athlon (TM) XP 1800+	1	AMD Athlon(TM) XP 1800+	671	648	Oct-0

IDEAS Top Performers - SPECint2000 (2003)

R	Company	System	#	Processor	Result	Basee	Date
1	Dell	Precision WorkStation 350 (3.06 GHz P4)	1	Intel Pentium 4 (533 MHz system bus)	1130	1085	Nov-02
2	Intel Corporation	Intel D850EMVR motherboard (3.06 GHz, Pentium 4 processor with HT Technology)	1	Intel Pentium 4 Processor with HT Technology (3.06 GHz, 533 MHz bus)	1107	1099	Aug-02
3	Dell	Precision WorkStation 340 (3.06 GHz P4)	1	Intel Pentium 4 (533 MHz system bus)	1074	1032	Nov-02
4	Dell	Precision WorkStation 350 (2.8 GHz P4)	1	Intel Pentium 4 (533 MHz system bus)	1061	1017	Nov-02
5	Intel Corporation	Intel D850EMVR motherboard (2.8 GHz, Pentium 4 processor)	1	Pentium 4 processor (2.8 GHz, 533 MHz bus)	1040	1032	Jul-02
6	Dell	Precision WorkStation 350 (2.66 GHz P4)	1	Intel Pentium 4 (533 MHz system bus)	1026	983	Nov-02
7	Fujitsu Siemens C	CELSIUS R610	1	Xeon processor (2.8 GHz, 533 MHz bus)	1016	967	Feb-03
8	Dell	Precision WorkStation 340 (2.8 GHz P4)	1	Intel Pentium 4 (533 MHz system bus)	1010	970	Sep-02
9	Intel Corporation	Intel D850EMVR motherboard (2.67 GHz, Pentium 4 processor)	1	Pentium 4 processor (2.67 GHz, 533 MHz bus)	1005	998	Jul-02

IDEAS Top Performers - SPECint2000 (March 2004)

Rank	Company	System	# CPU	Processor	Peak Result	Baseline	Test Date
1	Intel Corporation	Intel D875PBZ motherboard (AA-206) (3.4 GHz, Pentium 4 Processor with HT Technology Extreme Edition)	1	Intel Pentium 4 Processor with HT Technology Extreme Edition (3.4 GHz, 800 MHz bus)	1704	1666	Jan-04
2	Intel Corporation	Intel D875PBZ (AA-206) motherboard (3.2 GHz, Pentium 4 processor with HT Technology Extreme Edition)	1	Intel Pentium 4 Processor with HT Technology Extreme Edition (3.2 GHz, 800 MHz bus)	1620	1583	Sep-03
4	Dell	Precision Workstation 360 (3.2 GHz Pentium 4 Extreme Edition)	1	Intel Pentium 4 (800 MHz system bus)	1601	1570	Feb-04
5	Dell	Precision Workstation 650 (3.20 GHz Xeon, 2MB L3 Cache)	1	Intel Xeon (533 MHz system bus)	1563	1532	Jan-04
6	IBM Corporation	IBM x335 (3.2GHz, 533MHZ FSB)	1	Intel Xeon processor	1517	1481	Feb-04
8	Dell	Precision Workstation 360 (3.2 GHz Pentium 4 Extreme Edition)	1	Intel Pentium 4 (800 MHz system bus)	1503	1464	Nov-03
9	ION Computer Systems	SR2300WV2 (3.2GHz Xeon processor w. 2MB L3 cache)	1	Intel Xeon processor, 533MHz system bus	1455	1452	Feb-04
10	Advanced Micro Devices	ASUS SK8N Motherboard, AMD Opteron (TM) 148	1	AMD Opteron(TM) 148	1477	1405	Nov-03
20	Dell	Precision Workstation 360 (3.40 GHz Pentium 4)	1	Intel Pentium 4 (800 MHz system bus)	1369	1325	Jan-04

IDEAS Top Performers - SPECint2000 (March 2005)

Rank	Company	System	# CPU	Processor	Peak	Bass	Date
1	Intel Corporation	Intel(R) D925XECV2 motherboard (3.73 GHz, Intel(R) Pentium(R) 4 processor Extreme Edition supporting Hyper-Threading Technology)	1 core, 1 chip, 1 core/chip (Hyper-Threading Technology enabled)	Intel(R) Pentium(R) 4 processor Extreme Edition supporting Hyper-Threading Technology (3.73 GHz, 1066 MHz bus)	1796	1793	Dec-04
2	Advanced Micro Devices	MSI K8N Neo2 Platinum Motherboard, AMD Athlon (TM) 64 FX-55	1 core, 1 chip, 1 core/chip	AMD Athlon (TM) 64 FX-55 (ADAFX55DEI5AS)	1854	1750	Sep-04
3	Intel Corporation	Intel(R) D925XECV2 motherboard (3.6 GHz, Intel(R) Pentium(R) 4 processor 660 supporting Hyper-Threading Technology)	1 core, 1 chip, 1 core/chip (Hyper-Threading Technology enabled)	Intel(R) Pentium(R) 4 processor 660 supporting Hyper-Threading Technology (3.6 GHz, 800 MHz bus)	1718	1715	Nov-04

IDEAS Top Performers - SPECint2000 (February 2006)

	Company	System	#CPU	Processor	Result	Base-line	Test Date
1	Advanced Micro Devices	ASUS A8N-SLI Deluxe, AMD Athlon (TM) 64 FX-57	1 core, 1 chip, 1 core/chip	AMD Athlon (TM) 64 FX-57	1970	1862	Jun-05
2	Advanced Micro Devices	TYAN Tomcat K8E (S2865), AMD Opteron (TM) 154	1 core, 1 chip, 1 core/chip	AMD Opteron(TM) 154 (939-pin)	1956	1837	Aug-05
3	Hewlett-Packard Company	ProLiant DL385 (AMD Opteron (TM) 254)	1 core, 1 chip, 1 core/chip	AMD Opteron(TM) 254	1914	1817	Aug-05
4	Fujitsu Siemens Computers	CELSIUS H230, Intel Pentium M 780	1 core, 1 chip, 1 core/chip	Intel Pentium M 780 (2.26 GHz)	1839	1812	Jul-05

Multiprocessor systems

March 2001

IDEAS Top Performers - SPECint_rate2000

Rank	Company	System	# CPU	Processor	Result	Baseline
1	SGI	SGI Origin 3800 128X 400MHz R12k	128	R12000	511.0	479.0
2	SGI	SGI 2800 128X 400MHz R12k	128	R12000	477.0	459.0
3	SGI	SGI Origin 3800 64X 400MHz R12k	64	R12000	259.0	241.0
4	Compaq Computer Corporation	AlphaServer GS320 Model 6/731	32	Alpha 21264A	142.0	123.0
5	SGI	SGI Origin 3400 32X 400MHz R12k	32	R12000	130.0	121.0
6	SGI	SGI 2400 32X 400MHz R12k	32	R12000	125.0	115.0
7	Unisys	e-@ction Enterprise Server ES7000	32	Intel Pentium III Xeon 700 MHz	85.3	84.1
8	Fujitsu Limited	PRIMEPOWER800/1000/2000 (563MHz)	16	SPARC64 GP	70.4	61.9
9	Compaq Computer Corporation	AlphaServer GS160 Model 6/731	16	Alpha 21264A	69.9	63.1
10	SGI	SGI Origin 3400 16X 400MHz R12k	16	R12000	65.3	60.5
11	IBM Corporation	RS/6000 SP-375MHz High Node(16 CPU)	16	Power3-II	46.0	41.7
12	Unisys	e-@ction Enterprise Server ES7000	16	Intel Pentium III Xeon 700 MHz	44.3	43.5
13	Compaq Computer Corporation	AlphaServer GS80 Model 6/731	8	Alpha 21264A	36.0	33.0
14	IBM Corporation	RS/6000 SP-375MHz High Node(12 CPU)	12	Power3-II	34.6	31.4
15	Sun Microsystems	Sun Enterprise 4500	14	UltraSPARC-II	34.5	32.0
16	Hewlett Packard Corporation	HP 9000 Model N4000	8	552 MHz PA-RISC 8600	32.7	31.7
17	SGI	SGI Origin 3200 8X 400MHz R12k	8	R12000	32.6	30.3
18	Fujitsu Limited	PRIMEPOWER600 (500MHz)	8	SPARC64 GP	30.6	27.5
19	SGI	SGI 2200 8X 400MHz R12k	8	R12000	30.5	28.4
20	Fujitsu Limited	PRIMEPOWER600 (400MHz)	8	SPARC64 GP	25.2	22.6

IDEAS Top Performers - SPECint_rate2000

March 2002

Rank	Company	System	# CPU	Processor	Result	Baseline	Test Date
1	SGI	SGI Origin 3800 256X 500MHz R14k	256	R14000	1189	1150	Nov-01
2	SGI	SGI Origin 3800 128X 500MHz R14k	128	R14000	605	582	Nov-01
3	Fujitsu Limited	PRIMEPOWER2000 (675MHz)	128	SPARC64 GP	571	540	Sep-01
4	Fujitsu Siemens Computers	PRIMEPOWER2000 (675MHz)	128	SPARC64 GP	571	540	Sep-01
5	SGI	SGI Origin 3800 128X 400MHz R12k	128	R12000	511	479	Aug-00
6	SGI	SGI 2800 128X 400MHz R12k	128	R12000	477	459	May-00
7	Hewlett Packard Corporation	HP Superdome 64-way (750MHz PA-8700)	64	PA-8700	377	357	Aug-01
8	Fujitsu Limited	PRIMEPOWER2000 (675MHz)	64	SPARC64 GP	319	299	Sep-01
9	Fujitsu Siemens Computers	PRIMEPOWER2000 (675MHz)	64	SPARC64 GP	319	299	Sep-01
10	SGI	SGI Origin 3800 64X 500MHz R14k	64	R14000	307	296	May-01
11	SGI	SGI 2400 64X 500MHz R14k	64	R14000	289	278	Aug-01
12	Hewlett Packard	HP9000 Superdome 64-way (552MHz PA-8600)	64	PA-8600	272	258	Mar-01
13	SGI	SGI Origin 3800 64X 400MHz R12k	64	R12000	259	241	Jul-00
14	Compaq Computer Corporation	AlphaServer GS320 Model 32 68/1001	32	Alpha 21264C	218	200	Jun-01
15	Hewlett Packard Corporation	HP Superdome 32-way (750MHz PA-8700)	32	PA-8700	193	183	Sep-01

IDEAS Top Performers - SPECint_rate2000 (March 2003)

Rank	Company	System	#CPU	Processor	Result	Baseline	Test Date
1	SGI	SGI Origin 3800 256X 600MHz R14000A	256	R14000 A	1402	1344	Aug-02
2	SGI	SGI Origin 3800 256X 500MHz R14k	256	R14000	1189	1150	Nov-01
3	SGI	SGI Origin 3800 128X 600MHz R14k	128	R14000	714	693	Feb-02
4	SGI	SGI Origin 3800 128X 500MHz R14k	128	R14000	605	582	Nov-01
5	Fujitsu Limited	PRIMEPOWER2000 (675MHz)	128	SPARC64 GP	571	540	Sep-01
6	Fujitsu Siemens Computers	PRIMEPOWER2000 (675MHz)	128	SPARC64 GP	571	540	Sep-01
7	SGI	SGI Origin 3800 128X 400MHz R12k	128	R12000	511	479	Aug-00
8	SGI	SGI 2800 128X 400MHz R12k	128	R12000	477	459	May-00
9	Hewlett-Packard Company	HP Superdome 64-way (875MHz PA-8700+)	64	PA-8700+	413	394	Jun-02
10	Hewlett-Packard Company	HP Superdome 64-way (750MHz PA-8700)	64	PA-8700	377	357	Aug-01

IDEAS Top Performers - SPECint_rate2000 (March 2004)

Rank	Company	System	# CPU	Processor	Result	Baseline	Test Date
1	SGI	SGI Origin 3800 256X 600MHz R14000A	256	R14000A	1402	1344	Aug-02
2	SGI	SGI Origin 3800 256X 500MHz R14k	256	R14000	1189	1150	Nov-01
3	Hewlett-Packard Company	HP Integrity Superdome 64-way (1500 MHz Itanium 2)	64	Intel Itanium 2	904	904	Aug-03
4	SGI	SGI Altix 3000 (1500MHz, Itanium 2)	64	Intel Itanium 2		854	Sep-03
5	SGI	SGI Altix 3000 (1300MHz, Itanium 2)	64	Intel Itanium 2		705	Dec-03
6	SGI	SGI Origin 3800 128X 600MHz R14k	128	R14000	714	693	Feb-02
7	SGI	SGI Altix 3000 (1300MHz, Itanium 2)	64	Intel Itanium 2	601	601	Jun-03
8	SGI	SGI Origin 3800 128X 500MHz R14k	128	R14000	605	582	Nov-01

IDEAS Top Performers - SPECint_rate2000 (March 2005)

	Company	System	# CPU	Processor	R	B	Date
1	SGI	SGI Altix 3700 Bx2 (1600MHz 6M L3, Itanium 2)	128 cores, 128 chips, 1 core/chip	Intel Itanium 2		1956	Nov-04
2	SGI	SGI Altix 3000 (1500MHz, Itanium 2)	128 cores, 128 chips, 1 core/chip	Intel Itanium 2		1721	Apr-04
3	SGI	SGI Altix 3700 Bx2 (1500MHz, Itanium 2)	128 cores, 128 chips, 1 core/chip	Intel Itanium 2		1713	Dec-04
4	SGI	SGI Origin 3800 256X 600MHz R14000A	256	R14000A	1402	1344	Aug-02
5	SGI	SGI Origin 3800 256X 500MHz R14k	256	R14000	1189	1150	Nov-01
6	Hewlett-Packard	HP Integrity Superdome (1.6GHz/9MB Itanium 2, 16 cells)	64 cores, 64 chips, 1 core/chip	Intel Itanium 2 (1.6GHz/9MB, 400MHz FSB)	1108	1108	Jan-05
7	IBM	IBM eServer p5 595 (1900 MHz, 64 CPU)	64 cores, 32 chips, 2 cores/chip (SMT on)	POWER5	1147	1063	Oct-04
8	SGI	SGI Altix 3700 Bx2 (1600MHz 9M L3, Itanium 2)	64 cores, 64 chips, 1 core/chip	Intel Itanium 2		1052	Oct-04

Computer architectures

The processor

End

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