Computer architectures

The Buses

Általános
INFORMATIKAI
Tanszék

What will it be about?

- Buses and related concepts
- Characteristics of famous buses

- **Bus** (bus, buses):
  Circuits and wires that conduct data traffic between individual functional units .

The Bus

- Three types of routes are possible between the main sub-components:
  - Between processor and memory;
  - Between processor and I/O devices;
  - Between memory and I/O devices
- But the circuits and wires that carry out the data traffic between the individual smaller functional components are also called Buses: we can talk about the internal buses of a CPU, the wires on a printed circuit board are buses, etc.

The Bus

- **The bus: the set of circuits, wires and connectors that facilitate the flow of information between components (modules) and are necessary for system control.**
- **Functions:**
  - **To transport all bits of an n-bit word from a component connected to a bus to another component. Bits are mostly transferred in parallel.**
  - **They can be dedicated or split Buses: between two components or shared by several components (sharing!)**

The bus (bus) - history

- In the case of the initial main-frames, two wires "bundle" from the processor to the memory, or to the devices. The processor handled the two "worlds" with separate instructions, different timings, and protocols. At first, it is not an interruption (interrupt - IT) technique, but polling for the devices. Then IT emerged, with priorities. Daisy chain for peripherals. For multiprocessor systems, memory access is also solved with IT priorities.
- DEC's big idea: let the same bus handle both "worlds": UNIBUS
- Early PCs are also like this: The bus connected to the CPU legs leads to parallel sockets on the motherboard. Device control cards can be inserted into the sockets, memory chips into the memory socket. The CPU controls the bus. The controllers of the peripherals signal with IT, but the CPU "pushes" the data from their buffer into the memory.
- This simple bus system had a disadvantage: all components had to work at the same speed. Also: the bus could only be controlled by the CPU, instead of performing more useful tasks. Development: two worlds emerge: one is the CPU & memory, the other is the peripherals. Among them is the bus controller circuit. The CPU can work at a higher speed. The devices are able to communicate even without the supervision of the CPU, there is quite a lot of data transfer between the devices. The result was better overall performance. It was easier to build wider and wider (parallel) Buses, and to implement "plug-n-play" solutions instead of "setup" and "jumpering".
- The need for speed increased, the performance of the Buses brought starvation. The Buses were further "divided": SCSI, IDE, AGP, etc.

Bus classifications

- **Scope** (level).
  - **Local** Buses (usually non-standard, within a card, module, chip),
  - **System** Buses (between important system components, "backplane buses", mostly standard),
  - **I/O level** Buses (for connecting peripherals),
  - **intersystem** Buses (Buses connecting computers, usually standard, e.g. networks).
- The order of bit **transmission**
  - **Parallel buses** (each bit has its own line)
  - **Serial buses** (the lines carry a sequence of bits)

Bus classifications - in practice

- There can be **"internal" buses** that connect internal devices (e.g. memory, graphics card), and
- **"External" buses** for external devices (disks, scanner, camera, etc.). The internal Buses are sure to connect the components on the motherboard, while the device (controller) of the external bus can be on the motherboard or on an expansion card or port.
- **Parallel internal** buses: EISA, PCI, local buses
- **Serial internal**: 1-Wire, I^2C, SPI (Serial Peripheral Interface Bus), PCI Express, HyperTransport

- **Parallel external**: IDE (ATA), IEEE-488, PCMCIA (Personal Computer Memory Card Association), SCSI, Centronics parallel
- **Serial external**: USB, FireWire

Logic classes of bus (lines).

- **Data transfer dus**
  - **data bus,**
  - **address bus, address modifier bus.**

  (For these, an important characteristic is the bus width: the number of bits that can be transferred in parallel, the "number of lines")
- **Arbitration bus (helps to resolve the conflict)**
- **Interrupt and sync bus**
- **Service bus**

Logic classes of bus (lines). - another

- **Data bus** (Data Bus)
- **Address** Bus
- **Control bus** (Control Bus)
  - the **data transfer control**,
  - transmit **interrupts,**
  - controls **synchronization**,
  - transmits the **bus control signals** itself
- **Signals controlling** the data transfer can be:
  - the signal specifying the (memory - I/O) data transfer ***component ;***
  - ***read/write*** indication;
  - ***address strobe*** signal (indicates the stable state of the address);
  - ***data strobe*** indication (data bus bits are stable);
  - ***ready indication*** (the device is available - data transfer completed).

Terminology

- **Module, component**: device connected to the bus
- **Master** (active) module: able to initiate a bus operation and control the bus. There are potential masters.
- **Slave** (passive) module: able to respond
- **Bus reservation** (arbitration): a mechanism that selects one of those claiming the right to control the bus (since there can only be one master (controller) at a given time) .
- **Source** (transmitter) and **target** (receiver) module

If a slave module would like to be a source, it can only request the transfer (e.g. with interruption)

Terminology

- **Bus transaction**: sequence of activities (possibly time) between the occurrence of the bus request and the end of the transfer. It can include **several operations** (phases) (these may require several bus cycles):
  - **bus request,**
  - **bus reservation** (arbitration),
  - **addressing** (can be location-independent (individual), memory embedded and group),
  - **data transfer,**
  - **error detection and error indication,**
  - **termination of the master's right** .

  Protocol: rules for correct execution of a transaction. Rules related to timing, control, format, data representation.

Terminology

Component addressing can be:

- **Location-independent :**
  Each device has a clear, unique address, it is not necessary to select the component (or group);
- **Memory embedded addressing:**
  I/O is addressed as memory, there is no separate peripheral instructions (peripheral operation). The memory and I/O address range coincide.
- **Group addressing:**
  All passive units are addressed (e.g. reset all devices).

What does the bus standard mean?

- **Electrical specifications**
  - the number of data and address lines,
  - types and functions of control lines,
  - signal levels, signal level changes,
  - load capacity data, etc.
- **Mechanical specifications**
  - dimensions, connector types, connections, etc.
- **Timing specifications** etc.
- **Protocols.**

Let's note ...

- We often mark the buses with a line, but they are
  - circuits,
  - they also require time for signals to run.
  - They work in cycles and
  - levels (or level changes) appear after the transients.
- Electrical characteristics:
  - bus line drive circuits (bus drivers),
  - bus line receiver circuits,
  - transmission characteristics (finite signal propagation speed, distortions, etc.)
  - bus holder circuits (possibly),
  - power-down circuit (possibly).

Communication methods can be

- **Synchronous Buses** (transmission-reception at a given speed, with timed synchronization signals).
  - Devices connected to the bus **use the same clock signal** (clock edges) ;
  - Data is sent and received **at the same speed** ;
  - **connection always exists**, connect is not required;
  - **acknowledgement** is not required;
  - **fast**, but also requires line transmitting synchronisation;
- **Asynchronous transmission** (transmitter and receiver are not in sync, contact, acknowledgement of receipt is required).
  - **the speed of the components may be different**;
  - **no permanent connection**;
  - **acknowledgement can be done** by handshake.

Bus performance

- Depends on the clock speed and cycle time of the bus,
- the bit width of the bus,
- the transmission protocol,
- the number of bus controllers: the time of the arbitration algorithm.

(Arbitration: “competitive” assignment occurring in the case of more controllers.)

Control methods

- **Block transmission** (Burst Mode): data blocks are moving in a single bus operation.
- Dynamic **bus width change**
- **Protocol switching**

Basic concepts

- The two entities of the transfer are the *source* and the *destination*
- Any entity can be the *initiator*
  - Initiated by the source: writing;
    - Eg from CPU reg to mem. writing to a register
  - Initiated by the goal: reading
    - E.g. mem into CPU reg. reading from a register
- Conventional transmission:
  - Write : address1 + data1 + address2+ data2+ ...
  - Reading : address1 + address2+
    -data1 -data2

Block transfer

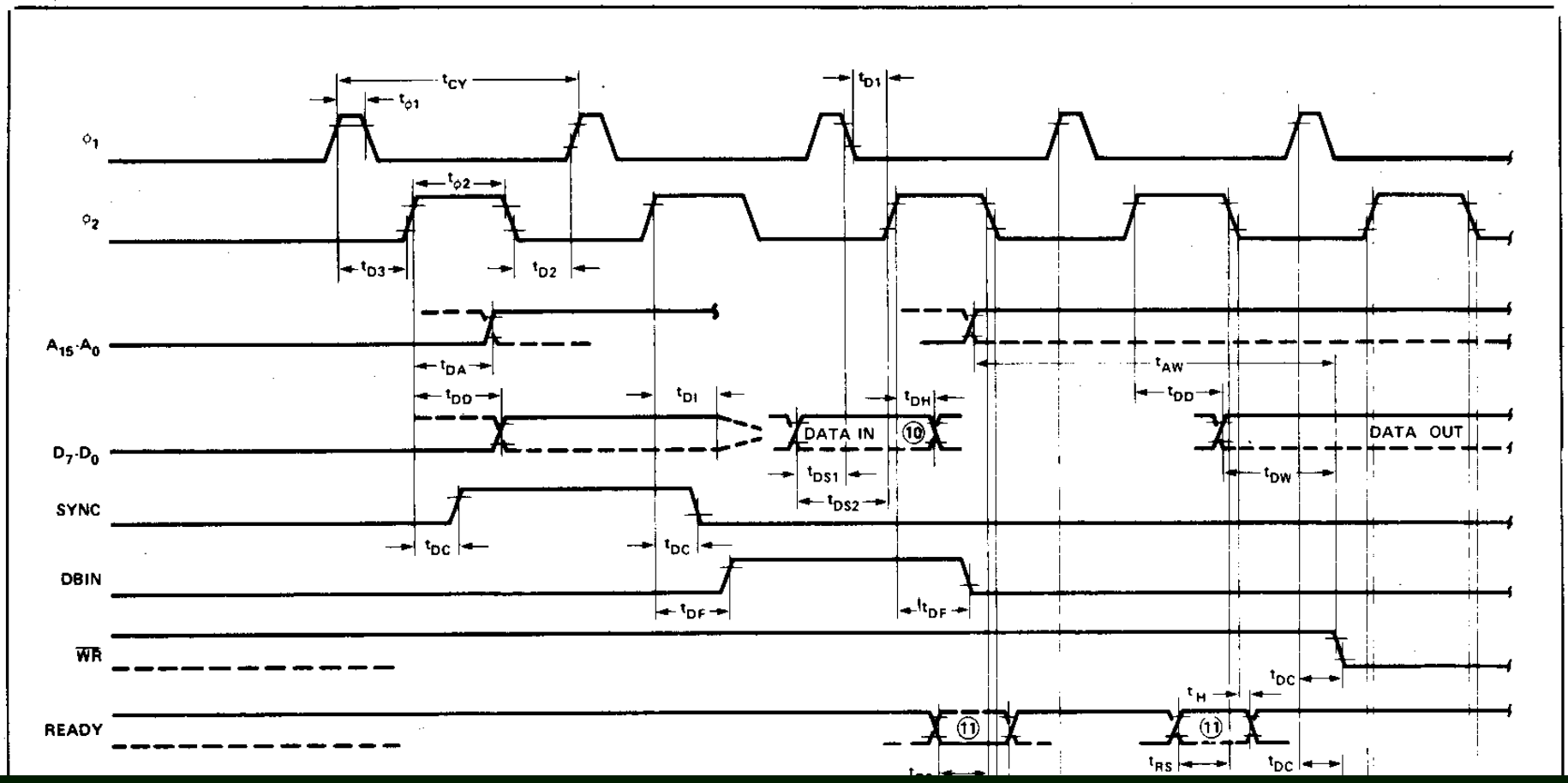
- **Writing :**
  - start address+data1+data2+data3+ ...
- **Reading :**
  - start address+
    -data1-data2-data3- ...
- "Saving" the address transfers ....
- consecutive addresses at the source,
- at the destination, the data comes/goes to consecutive addresses ...

Reading, writing

intel

8080A/8080A-1/8080A-2

WAVEFORMS

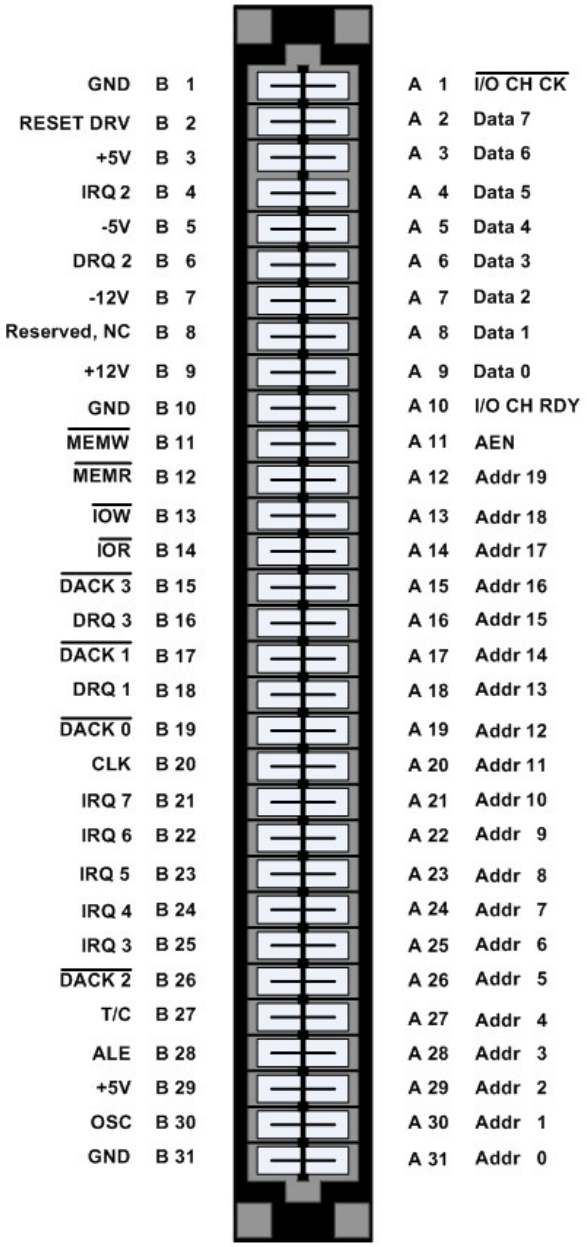


Famous Buses

- **PC XT (1981)** (XT: Extended Technology)
  - **8-bit data, 20-bit address, 7 interrupt requesting lines, 4 direct memory access lines,**
  - **4.77 MHz frequency, synchronous**
  - **can be only controlled by CPU and DMA on the motherboard,**
  - **open standard.**
- **PC AT (1984)** (AT: Advanced Technology) , **later ISA** (ISA: Industry Standard Architecture)
  - **16-bit data (but also 8-bit cards), 24-bit address, 15 interrupt requests, 8 direct memory access request lines, 6 - 12.4 MHz clock frequency,**
  - **can also be controlled by an external unit,**
  - **open standard.**

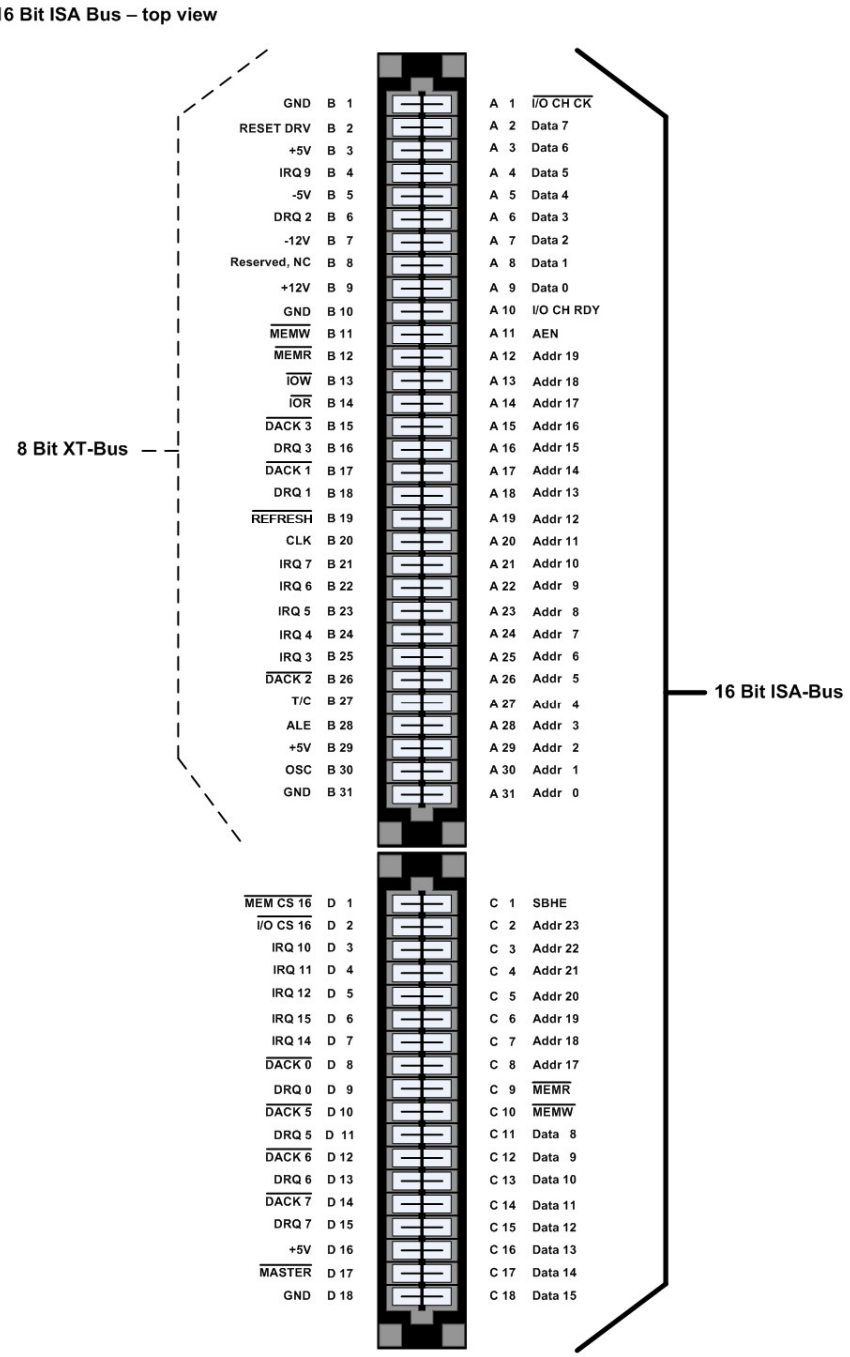
ISA 8bit

8 Bit XT Bus – top view



GND	B	1	A	1	$\overline{\text{I/O CH CK}}$
RESET DRV	B	2	A	2	Data 7
+5V	B	3	A	3	Data 6
IRQ 2	B	4	A	4	Data 5
-5V	B	5	A	5	Data 4
DRQ 2	B	6	A	6	Data 3
-12V	B	7	A	7	Data 2
Reserved, NC	B	8	A	8	Data 1
+12V	B	9	A	9	Data 0
GND	B	10	A	10	I/O CH RDY
$\overline{\text{MEMW}}$	B	11	A	11	AEN
$\overline{\text{MEMR}}$	B	12	A	12	Addr 19
$\overline{\text{IOW}}$	B	13	A	13	Addr 18
$\overline{\text{IOR}}$	B	14	A	14	Addr 17
$\overline{\text{DACK 3}}$	B	15	A	15	Addr 16
DRQ 3	B	16	A	16	Addr 15
$\overline{\text{DACK 1}}$	B	17	A	17	Addr 14
DRQ 1	B	18	A	18	Addr 13
$\overline{\text{DACK 0}}$	B	19	A	19	Addr 12
CLK	B	20	A	20	Addr 11
IRQ 7	B	21	A	21	Addr 10
IRQ 6	B	22	A	22	Addr 9
IRQ 5	B	23	A	23	Addr 8
IRQ 4	B	24	A	24	Addr 7
IRQ 3	B	25	A	25	Addr 6
$\overline{\text{DACK 2}}$	B	26	A	26	Addr 5
T/C	B	27	A	27	Addr 4
ALE	B	28	A	28	Addr 3
+5V	B	29	A	29	Addr 2
OSC	B	30	A	30	Addr 1
GND	B	31	A	31	Addr 0

ISA 16bit


16 Bit ISA Bus – top view
8 Bit XT-Bus
16 Bit ISA-Bus
GND B 1
RESET DRV B 2
+5V B 3
IRQ 9 B 4
-5V B 5
DRQ 2 B 6
-12V B 7
Reserved, NC B 8
+12V B 9
GND B 10
MEMW B 11
MEMR B 12
IOW B 13
IOR B 14
DACK 3 B 15
DRQ 3 B 16
DACK 1 B 17
DRQ 1 B 18
REFRESH B 19
CLK B 20
IRQ 7 B 21
IRQ 6 B 22
IRQ 5 B 23
IRQ 4 B 24
IRQ 3 B 25
DACK 2 B 26
T/C B 27
ALE B 28
+5V B 29
OSC B 30
GND B 31
A 1 I/O CH CK
A 2 Data 7
A 3 Data 6
A 4 Data 5
A 5 Data 4
A 6 Data 3
A 7 Data 2
A 8 Data 1
A 9 Data 0
A 10 I/O CH RDY
A 11 AEN
A 12 Addr 19
A 13 Addr 18
A 14 Addr 17
A 15 Addr 16
A 16 Addr 15
A 17 Addr 14
A 18 Addr 13
A 19 Addr 12
A 20 Addr 11
A 21 Addr 10
A 22 Addr 9
A 23 Addr 8
A 24 Addr 7
A 25 Addr 6
A 26 Addr 5
A 27 Addr 4
A 28 Addr 3
A 29 Addr 2
A 30 Addr 1
A 31 Addr 0
MEM CS 16 D 1
I/O CS 16 D 2
IRQ 10 D 3
IRQ 11 D 4
IRQ 12 D 5
IRQ 15 D 6
IRQ 14 D 7
DACK 0 D 8
DRQ 0 D 9
DACK 5 D 10
DRQ 5 D 11
DACK 6 D 12
DRQ 6 D 13
DACK 7 D 14
DRQ 7 D 15
+5V D 16
MASTER D 17
GND D 18
C 1 SBHE
C 2 Addr 23
C 3 Addr 22
C 4 Addr 21
C 5 Addr 20
C 6 Addr 19
C 7 Addr 18
C 8 Addr 17
C 9 MEMR
C 10 MEMW
C 11 Data 8
C 12 Data 9
C 13 Data 10
C 14 Data 11
C 15 Data 12
C 16 Data 13
C 17 Data 14
C 18 Data 15

Famous buses...

- **EISA (Extended Industry Standard Architecture)**
  - specified by several (9) companies,
  - 32/32-bit (but also accepts 8/16-bit cards), multi-master, burst mode transmission,
  - open standard with precise timing specifications,
  - 8 MHz, 32 MB/s
- **IBM MCA (Micro Channel Architecture) (1987)**
  - (16) 32/32 bits, 10 MHz,
  - not compatible with ISA, EISA Buses,
  - software configuration,
  - **not an open standard!**

The PCI bus

Led by Intel: Peripheral Component Interconnect

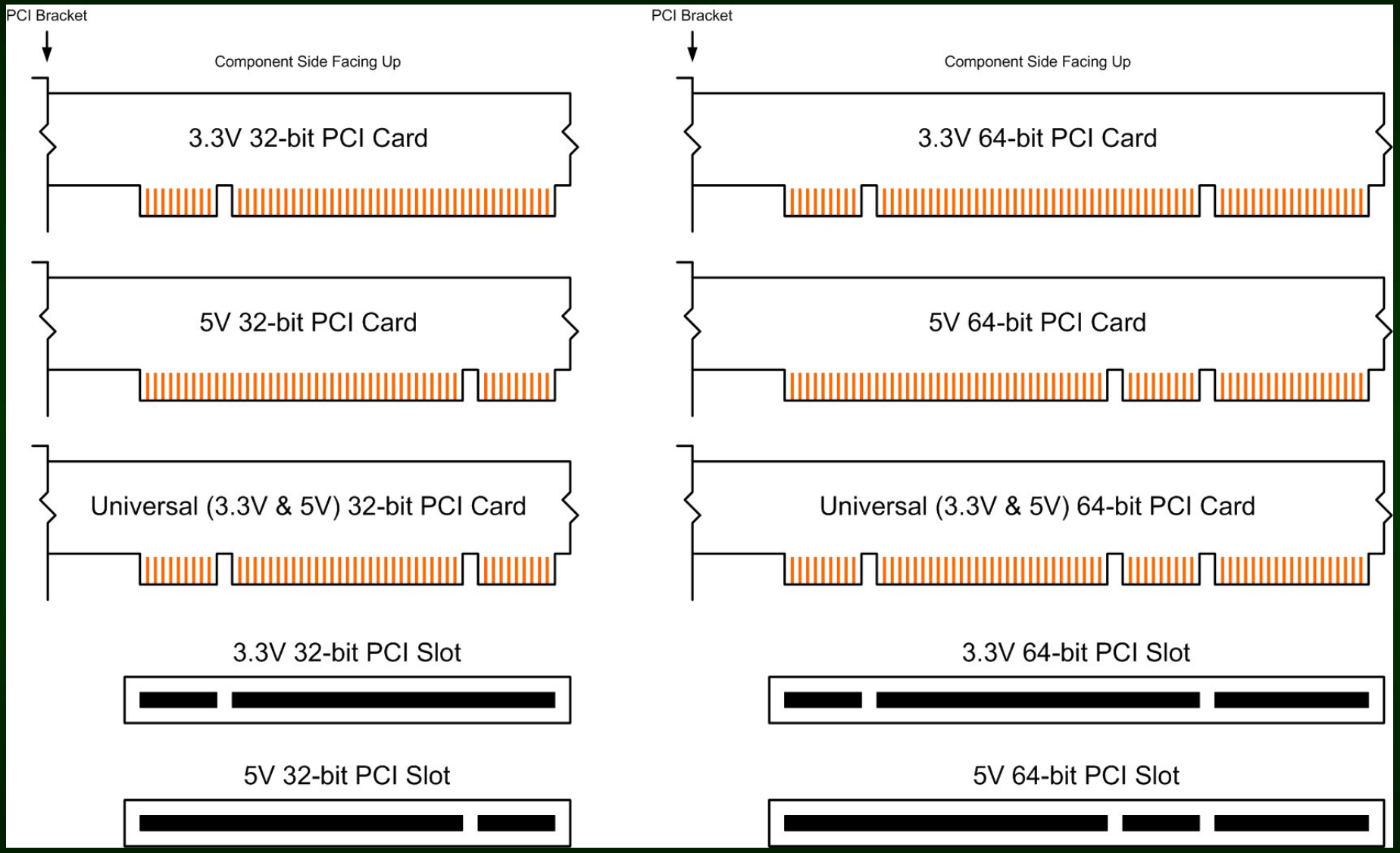
(1992, 93:2.0, 95: PCI 2.1)

- **Synchronous bus; 5 (or 3.3) V extension connectors;**
- **First: 32 bits, 33 MHz, (4*33=132 MB/s)**
- **PCI 2.0: 64-bit, 33 MHz**
- **PCI 2.1: 64 bit, 66 MHz (524 MB/s theoretically).**
- **PCI-X: 133MHz (1066MB/s)**
- **PCI-X 2.0: 266MHz, larger configuration memory (2133 MB/s)**
- **There are no separate address and data wires!**
  Losses are higher with non-block transmission!
- **Practically 50-80% performance.**
  - **From 1995-96, its distribution widens, until 2000 approx. same as ISA-EISA bus.**
  - **From 95, Apple replaces the NuBus bus with PCI.**
  - **In 2004, its serial version appeared: PCI Express**
  - **Other versions: Mini PCI, for laptops**

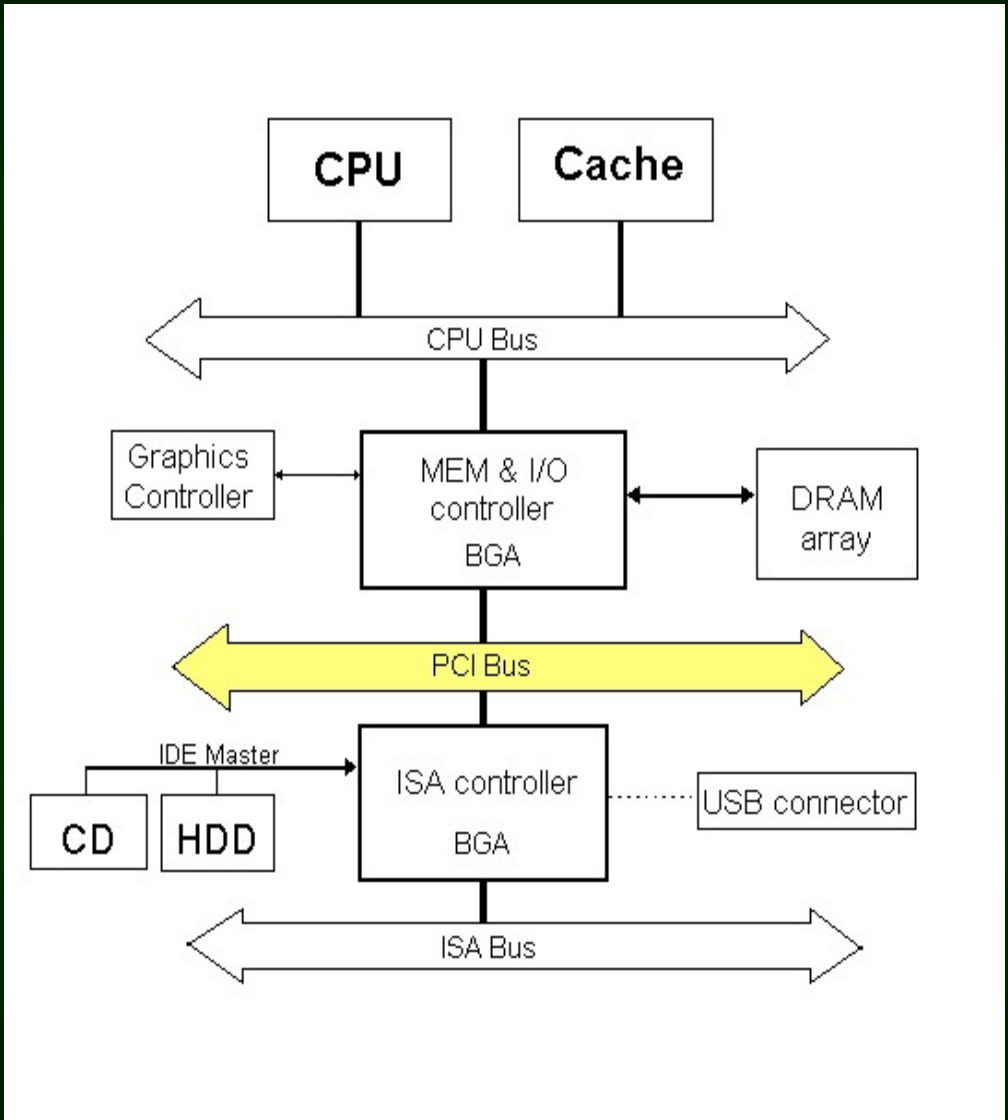
The PCI bus

- Additional benefits:
  - compatibility with 32-bit peripherals,
  - processor independent!
  - There is no need to "setup" the cards!
  - Shared connectors too! (This was important until 2000!)
- Many companies use it, even abandoning their own bus concept. For both client machines and servers!

PCI

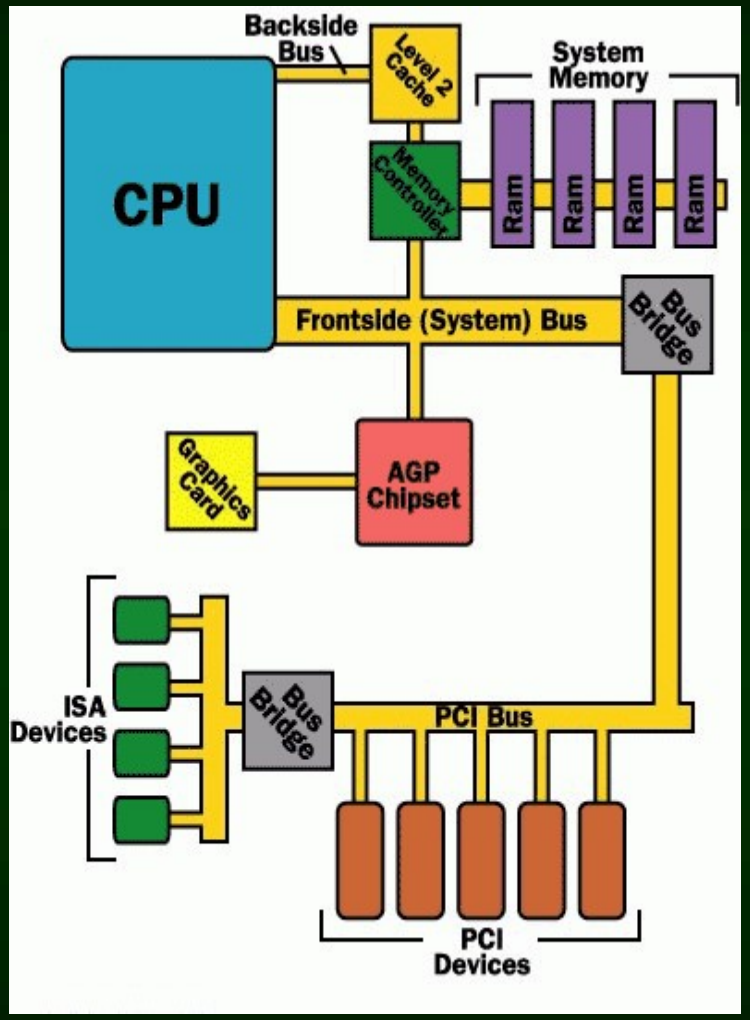

PCI Bracket
Component Side Facing Up
3.3V 32-bit PCI Card
5V 32-bit PCI Card
Universal (3.3V & 5V) 32-bit PCI Card
3.3V 32-bit PCI Slot
5V 32-bit PCI Slot
PCI Bracket
Component Side Facing Up
3.3V 64-bit PCI Card
5V 64-bit PCI Card
Universal (3.3V & 5V) 64-bit PCI Card
3.3V 64-bit PCI Slot
5V 64-bit PCI Slot

Architecture based on PCI bus



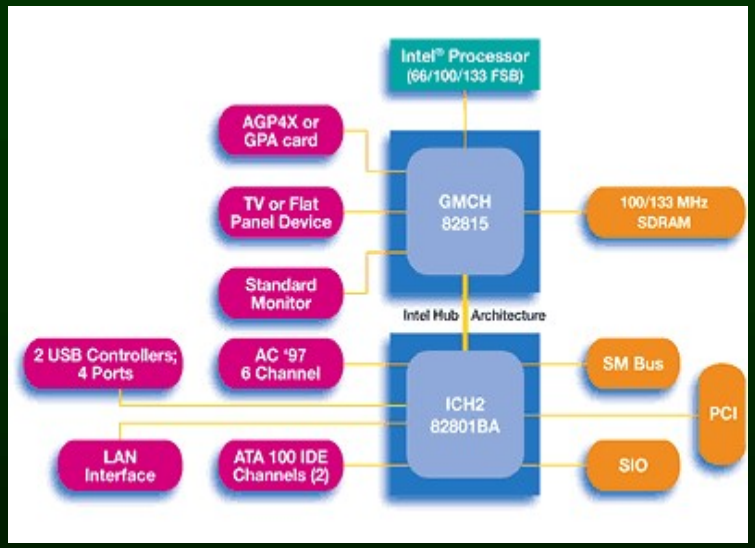
The so-called PCI *mezzanine* bus: located between the CPU bus and the system bus.

The bus systems of a "modern" PC...



Today, PCI bandwidth is no longer enough for graphics.
Intel: Mid 90s:
AGP (Accelerated Graphic Port)
From 2004, the serial version of PCI: PCI Express

… and a functional block diagram of the Intel 815 chipset …



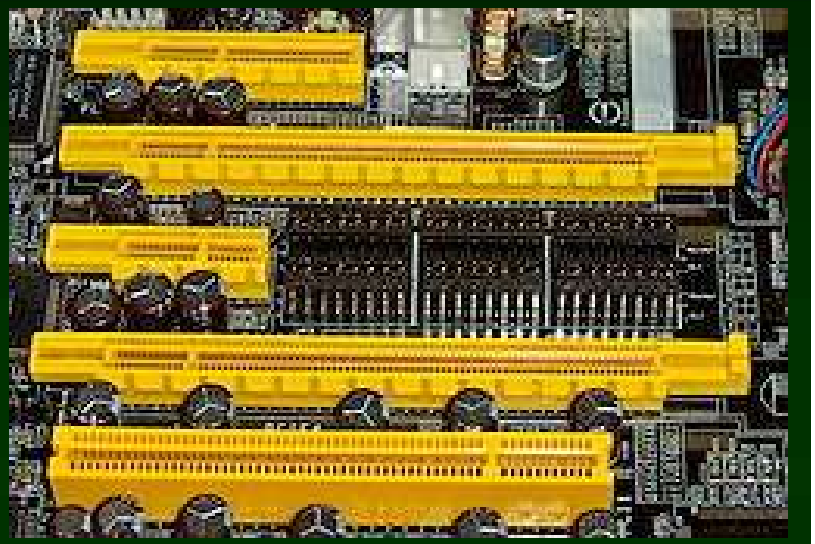
PCI Express

- Between 1991 and 2004, the PCI was valid
  - From 1997, the AGP "helped out"
- Demand continued to grow
- PCIe : on both Intel and AMD motherboards
  - serial, point-to-point bus
  - Scalable (lane: 4 pin width data paths can be multiplied)
  - x1, x4, x8, x16, x32

PCIe	Lanes	Pins	MB/s	Purpose
x1	1	4	500 MB/s	Device
x2	2	8	1000 MB/s = 1 GB/s	Device
x16	16	64	8000 MB/s = 8 GB/s	Graphics Card

PCI Express x4

Pin	Side B	Side A	Comments
1	+12V	PRSNT1#	Pulled low to indicate card inserted
2	+12V	+12V	
3	Reserved	+12V	
4	Ground	Ground	
5	SMCLK	TCK	
6	SMDAT	TDI	
7	Ground	TDO	SMBus and JTAG port pins
8	+3.3V	TMS	
9	TRST#	+3.3V	
10	+3.3 Vaux	+3.3V	Standby power
11	WAKE#	PWRGD	Link reactivation, power good.
Key notch			
12	Reserved	Ground	
13	Ground	REFCLK+	Reference clock differential pair
14	HSOp(0)	REFCLK-	Lane 0 transmit data, + and −
15	HSOn(0)	Ground	
16	Ground	HSIP(0)	Lane 0 receive data, + and −
17	PRSNT2#	HSIn(0)	
18	Ground	Ground	
19	HSO(1)	Reserved	Lane 1 transmit data, + and −
20	HSOn(1)	Ground	
21	Ground	HSIP(1)	Lane 1 receive data, + and −
22	Ground	HSIn(1)	
23	HSOp(2)	Ground	Lane 2 transmit data, + and −
24	HSO(2)	Ground	
25	Ground	HSIP(2)	Lane 2 received data, + and −
26	Ground	HSIn(2)	
27	HSOp(3)	Ground	Lane 3 transmit data, + and −
28	HSOn(3)	Ground	
29	Ground	HSIp(3)	Lane 3 received data, + and −
30	Reserved	HSIn(3)	
31	PRSNT2#	Ground	
32	Ground	Reserved	



x4,
×16,
×1 ,
×16 ,
32-bit PCI

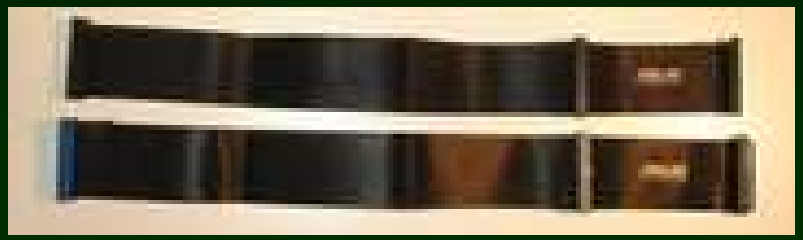
Other famous Buses: ATA

- **Advanced Technology Attachment: for external parallel bus disks, CD-ROM connection**
- **Acronyms: IDE (Integrated Drive Electronic), EIDE (Enhanced IDE), ATAPI (ATA Packet Interface), UDMA (Ultra Direct Memory Access).**
- **Serial ATA was introduced in 2003 , the name PATA (Parallel ATA) was retroactively given**

- **Reasons for size limits (504 MB, 8 GB, 32 GB, 137 GB):**
  - The original ATA specification used 28-bit addressing.
  - This would have allowed 137GB, but the standard BIOS of the time could only handle 8 GB. But the situation was worse, bringing the IDE and BIOS to the common denominator with the then CHS (Cylinder-Head-Sector) addressing gave only 512MB. LBA (Logical Block Addressing 48 bits) introduced system, the limit could already rise to 8GB. It could then rise over time.

ATA

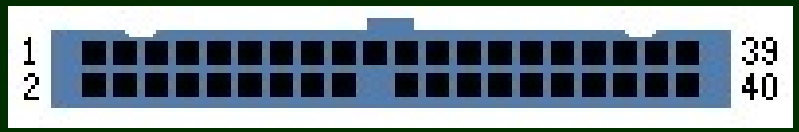
- 40-pin connectors (three) on a 40-line flat cable (with the appearance of UDMA, the cable has 80 wires, but the connector is 40).
- Cable max. 46 cm long: this makes it difficult to assemble large systems
- One cable can have a master and a slave device (device 0 and device 1)



- The device driver of the OS "manages" the arbitration: if device 1 executes a "command", device 0 cannot start a command (a slower CD can slow down the HD next to it)
- The ATA controller is on the motherboard.
  Two channels (channell): primary and secondary

ATA

Pin 1	Reset
Pin 2	Ground
Pin 3	Data 7
Pin 4	Data 8
Pin 5	Data 6
Pin 6	Data 9
Pin 7	Data 5
Pin 8	Data 10
Pin 9	Data 4
Pin 10	Data 11
Pin 11	Data 3
Pin 12	Data 12
Pin 13	Data 2
Pin 14	Data 13
Pin 15	Data 1
Pin 16	Data 14
Pin 17	Date 0
Pin 18	Data 15
Pin 19	Ground
Pin 20	Key or VCC_in
Pin 21	DDRQ
Pin 22	Ground
Pin 23	I/O write
Pin 24	Ground
Pin 25	I/O read
Pin 26	Ground
Pin 27	IOCHRDY
Pin 28	Cable selection
Pin 29	DDACK
Pin 30	Ground
Pin 31	IRQ
Pin 32	No connection
Pin 33	Addr 1
Pin 34	GPIO_DMA66_Detect
Pin 35	Addr 0
Pin 36	Addr 2
Pin 37	Chip select 1P
Pin 38	Chip select 3P
Pin 39	Activity
Pin 40	Ground



ATA standards and features

Name	Another name	**New features**	**ANSI Reference**
ATA-1	ATA, HERE	up to 528 MB	X3.221-1994 (obsolete since 1999)
ATA-2	EIDE, Fast ATA, Fast IDE, Ultra ATA	24-bit LBA (up to 8.4 GB)	X3.279-1996 (obsolete since 2001)
ATA-3	EIDE	28-bit LBA (up to 137 GB) SMART, Security	X3.298-1997 (obsolete since 2002)
ATA-4	ATAPI-4, ATA/ATAPI-4	Support for CD-ROM, etc., via ATAPI packet commands	NCITS 317-1998
ATA-5	ATA/ATAPI-5	80-wire cables	NCITS 340-2000
ATA-6	ATA/ATAPI-6	48-bit LBA (up to 144 TB) Automatic Acoustic Management	NCITS 347-2001
ATA-7	ATA/ATAPI-7	--	NCITS 361-2002
ATA-8	ATA/ATAPI-8	--	in project

1.0 SATA: 150Mbps, 2.0 SATA: 300Mbps

Serial ATA (SATA)

Serial ATA *(Serial Advanced Technology Attachment)*

- **SATA revision 1.0 (SATA 1.5 Gbit/s), (SATA/150), 2003 :**
  - **1.5 Gbit/s (8b/10b encoding overhead)**
  - **max. uncoded transfer rate 1.2 Gbit/s (150 MB/s)**
  - **SATA/150 ≈ SATA/133**
- **SATA revision 2.0 (SATA 3 Gbit/s), (SATA/300), 2004 :**
  - **3 Gbit/s**
  - **max. uncoded transmission speed 2.4 Gbit/s (300 MB/s)**
  - **SATA/150 compatible**
- **SATA revision 3.0 (SATA 6 Gbit/s), (SATA/600), 2008 :**
  - **6 Gbit/s, max. uncoded transmission speed 4.8 Gbit/s (600 MB/s)**
- **SATA revision 3.2 (SATA 16 Gbit/s), (SATA/1600), 2013 :**
  - **16 Gbit/s, max. unencoded transfer rate 1969 MB/s**

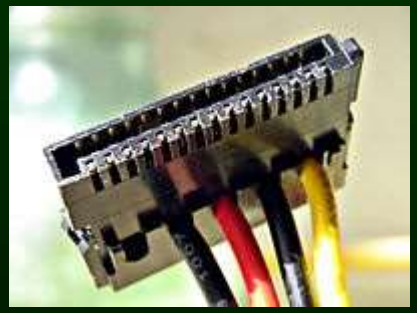
Serial ATA (SATA)

Serial ATA *(Serial Advanced Technology Attachment)*

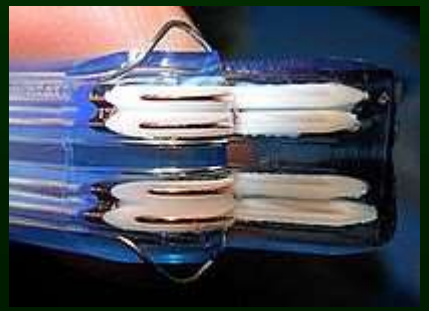
Pin #	Function
1	Grounding
2	A+
3	A−
4	Grounding
5	B−
6	B+
7	Grounding

Pin #	Function
1–3	3.3V
4–6	Grounding
7–9	5V
10	Grounding
11	Delayed start (only in supported drives)
12	Grounding
13–15	12V

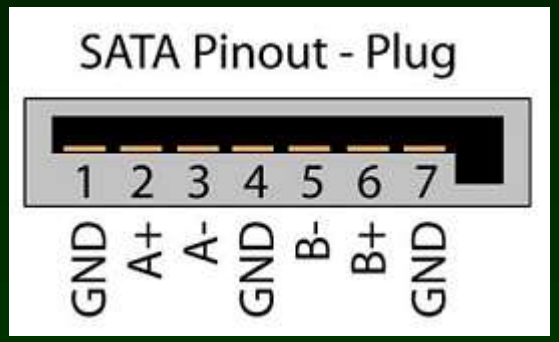
Hot swap

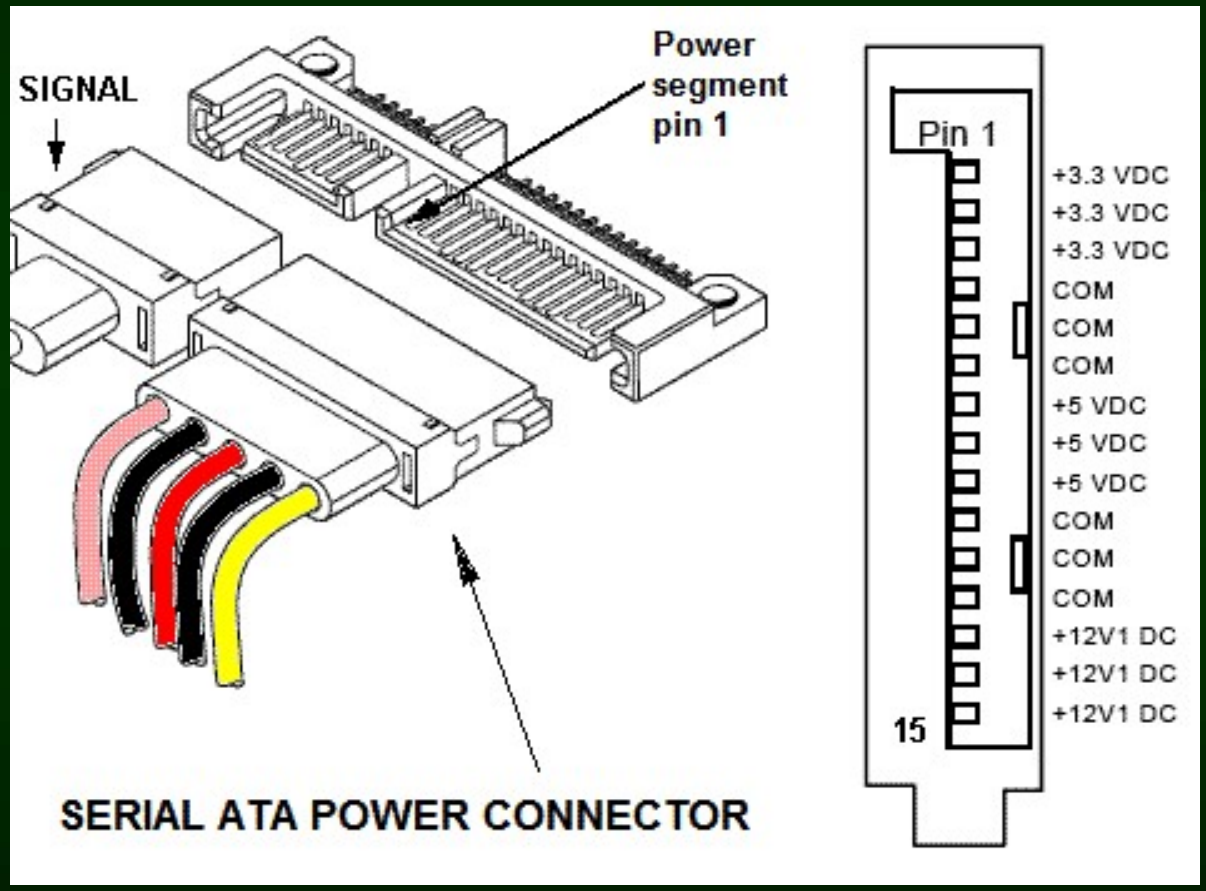


max. 1m cable

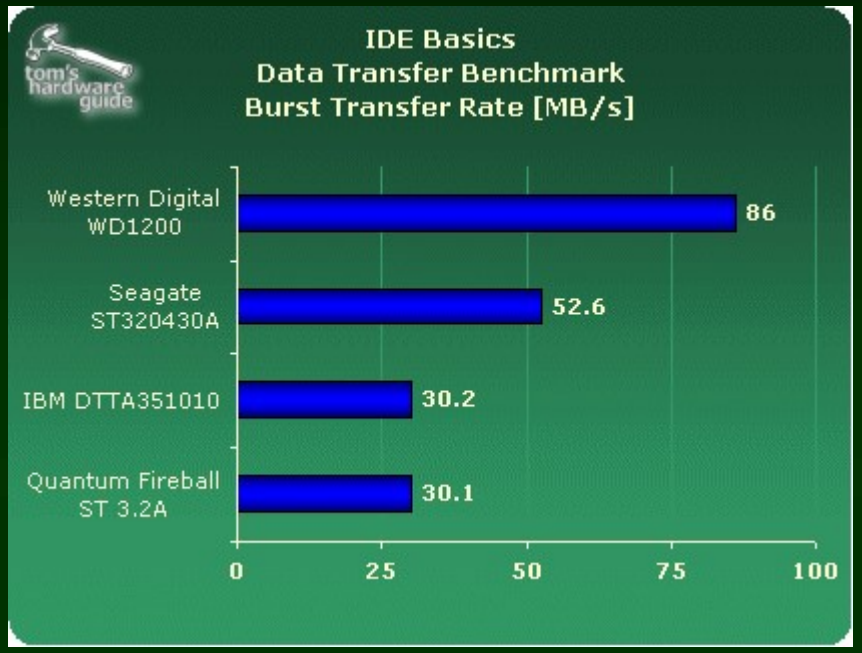


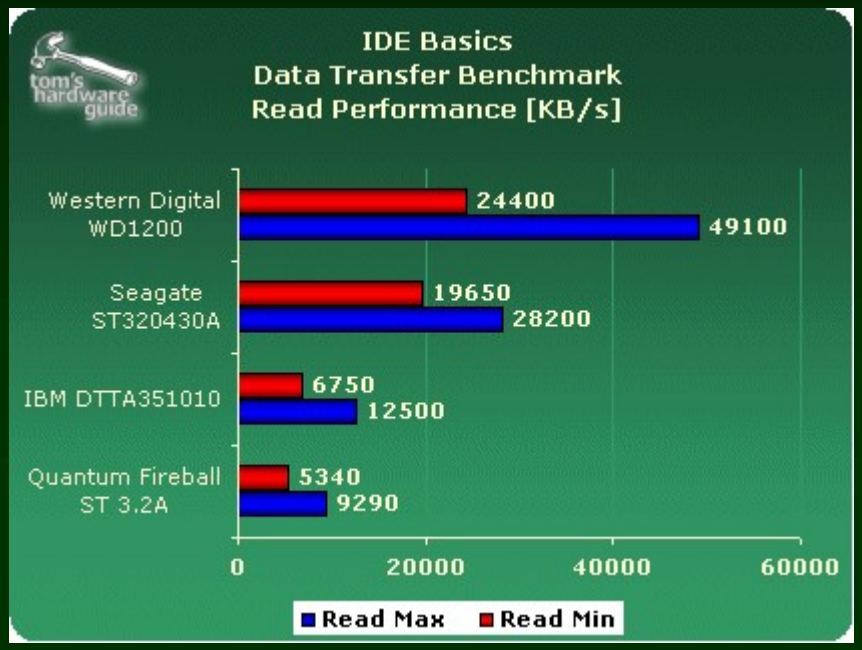
Serial ATA (SATA)





Something about performance...





http://www.tomshardware.com/storage/20020806/ide-08.html#benchmarks

2010 : 10,000 rpm SATA hard disk maximum data transfer rate up to 157 MB/s

2015 : disk hardware : 0.7-1.3 MB/s , SSD : 25-70 MB/s , cache : 200-400 MB/s

2022: NVMe SSD Sequential Read 7000 MB/s Sequential Write 5000 MB/s
Random Read 1000 MB/s Random Write 700 MB/s

non-volatile memory, PCI Express bus

Solid-state drive (SSD), Solid-state hybrid drive (SSHD)

More famous Buses

- **SCSI (Small Computer System Interface) (from 1981)**
  - SCSI-1 (1986)
  - SCSI-2 (Wide, Fast SCSI) (1989)
  - SCSI-3 (1992)
- **Max. 8 (16) devices can be connected (but only 2 can communicate)**
  - **initiator (can be the computer) and the target device (this can be a peripheral or even another machine),**
  - **(multi-master arbitration).**
  - **Cable length: 6m (25 m), 50-pin connectors.**

SCSI interface summary

Interface	Bit width	Clock signal	bus bandwidth	Max. cable length	Max. number of devices
SCSI	8 bits	5 MHz	5 MB/s	6 m	8
Fast SCSI	8 bits	10 MHz	10 MB/s	1.5-3m	8
Wide SCSI	16 bits	10 MHz	20 MB/s	1.5-3m	16
Ultra SCSI	8 bits	20 MHz	20 MB/s	1.5-3m	5-8
Ultra Wide SCSI	16 bits	20 MHz	40 MB/s	1.5-3m	5-8
Ultra2 SCSI	8 bits	40 MHz	40 MB/s	12 m	8
Ultra2 Wide SCSI	16 bits	40 MHz	80 MB/s	12 m	16
Ultra3 SCSI	16 bits	40 MHz DDR	160 MB/s	12 m	16
Ultra-320 SCSI	16 bits	80MHz DDR	320 MB/s	12 m	16

Another famous bus: USB

- **Universal Serial Bus**
  - **USB control and distribution (hub) system on the host (devices can be connected in a tree structure, max. 5 depth)**
  - **Also power supply on 5 m cable**
- **Advanced plug-n-play capabilities**
- **Many types of devices can be connected** (mouse, keyboard, scanner, camera, printer, HD, flash memory, network, etc.) **device classes**

USB device classes

USB Human interface device class:
mouse, keyboard *(Low Speed Rate: 1.5 Mbps)*
USB Mass storage device class:
Keydrives, HD, Cards, cameras, audio players
(***Full Speed Rate: 12 Mbps,***
or *Hi-Speed Rate: 480 Mbps* **)**
USB communication devices class (CDC):
modem, network cards, ISDN, Fax
USB printer device class:
USB audio device class:
sound card type device
USB video device class:
webcam, video cam

USB

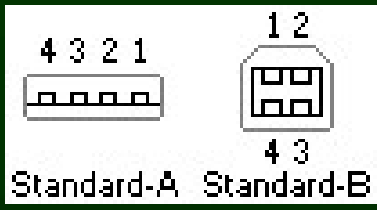
- Devices are connected to the host (host controller) via the USB bus
- Tools functions. The hub has no official function
  - All devices/functions are identified
- The endpoint: the function away from the host
- A pipe is formed from the host to the endpoint.
  32 active channels for endpoints: 16 inward,
  16 outward (in and out are defined from the host's point of view)
- Packag sizes are varying on the channels

USB

- 4 data transmission types on the channels
  - *Control*. Bidirectional, commands to the device, status information to the host
  - *Interruption*. One-way transmission, for devices that require fast reactions (mouse, keyboard, joystick)
  - *Isochron*. One-way, guaranteed speed devices where a package can be lost (telephone, speaker, realtime video, etc.)
  - *Bulk*. Two-way, for transferring large amounts of data, no delay guarantee, but with acknowledgement (file transfer)

USB

- Three transmission speeds
  - **Low Speed Rate** : 1.5 Mbps.
    Mainly for HiD (Human Interface Devices).
  - **Full Speed Rate** : 12 Mbps.
    Before USB 2.0, this was the maximum
  - **Hi-Speed Rate** : 480 Mbps. Only from USB 2.0.
- The USB connectors
  - Type A and B, not interchangeable (no circle)
  - 4 wires (Power, D+, D-, Earth).
    Twisted pair, shielded is better.
  - Power: 5 V, 500 mA. It may not be enough for a device that requires high performance



USB versions

- USB 1.0 FDR Nov 1995
- USB 1.0 Jan 1996
- USB 1.1 Sep 1998
- USB 2.0 Apr 2000
  - HI- Speed Mode
- USB 2.0 revised Dec. 2002
  - All three rates, backwards compatibility
- USB 3.0 2008
  - 5 Gbps (1.5A (5V, 7.5W) , 5A (20V, 100W) Battery Charging Specification)
- USB 3.1 2013
  - 10 Gbps
- USB 3.2 2017
  - 20 Gbps
- USB 4 2019 only USB C
  - 20 Gbps DisplayPort and PCI Express tunneling

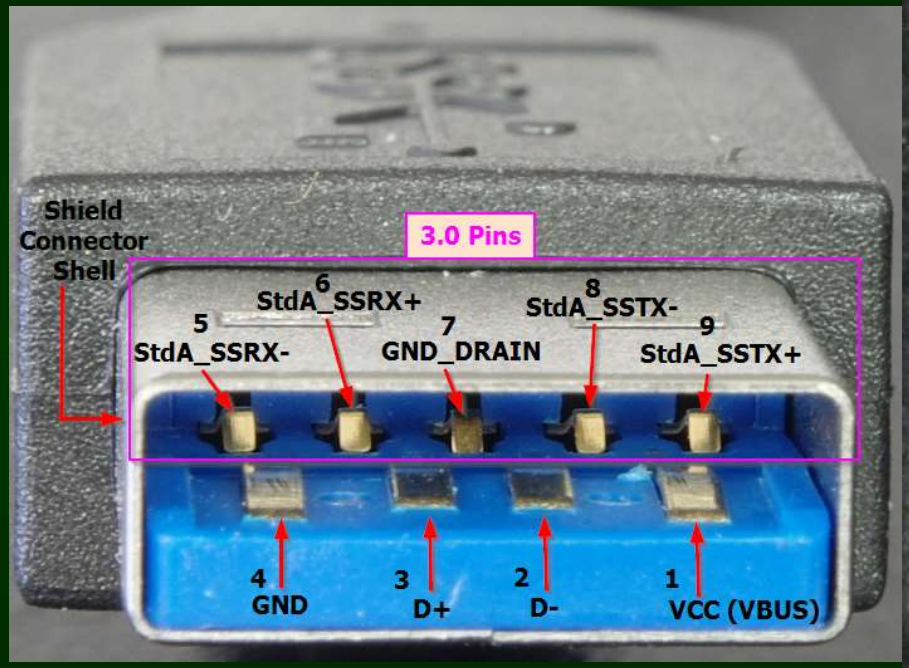
USB versions : USB 3.0

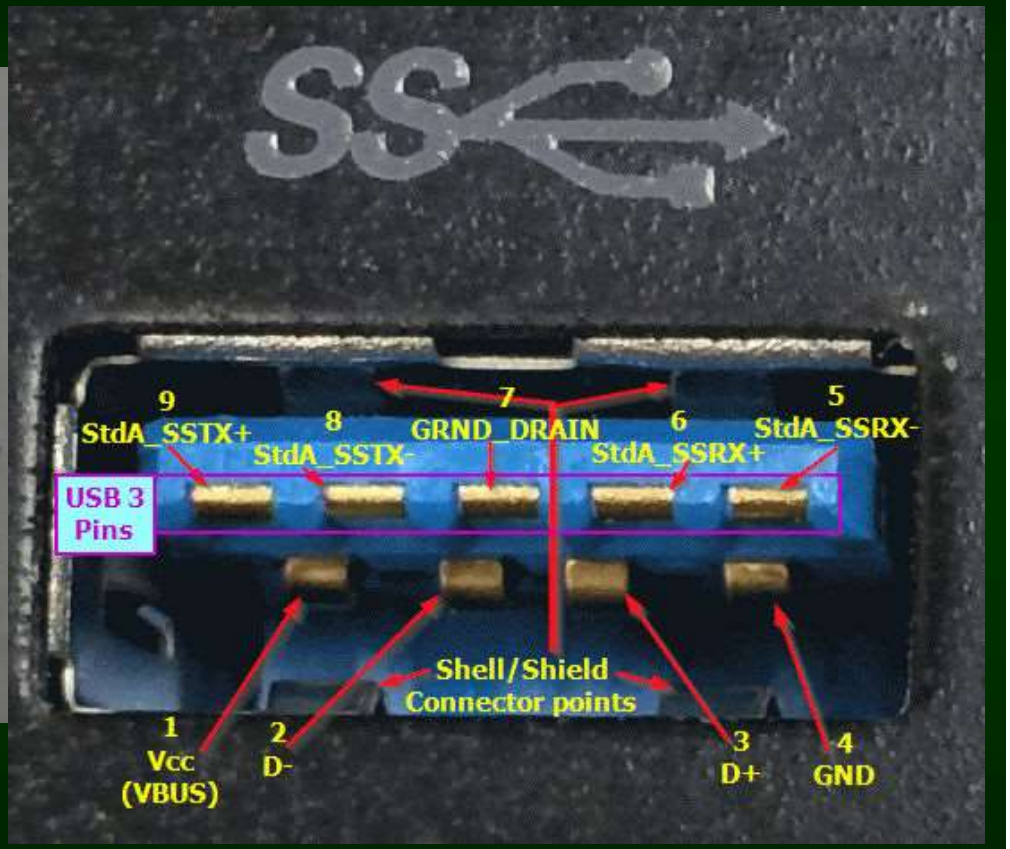
USB 3.0 connector pinouts[51]

Pin	Color	Signal name		Description
		A connector	B connector	
Shell	N/A	Shield		Metal housing
1	Red	VBUS		Power
2	White	D−		USB 2.0 differential pair
3	Green	D+		
4	Black	GND		Ground for power return
5	Blue	StdA_SSRX−	StdB_SSTX−	SuperSpeed receiver differential pair
6	Yellow	StdA_SSRX+	StdB_SSTX+	
7	N/A	GND_DRAIN		Ground for signal return
8	Purple	StdA_SSTX−	StdB_SSRX−	SuperSpeed transmitter differential pair
9	Orange	StdA_SSTX+	StdB_SSRX+	
The USB 3.0 *Powered-B* connector has two additional pins for power and ground supplied to the device.[52]				
10	N/A		DPWR	Power provided to device (Powered-B only)
11			DGND	Ground for DPWR return (Powered-B only)

https://en.wikipedia.org/wiki/USB_3.0

USB versions : USB 3.0





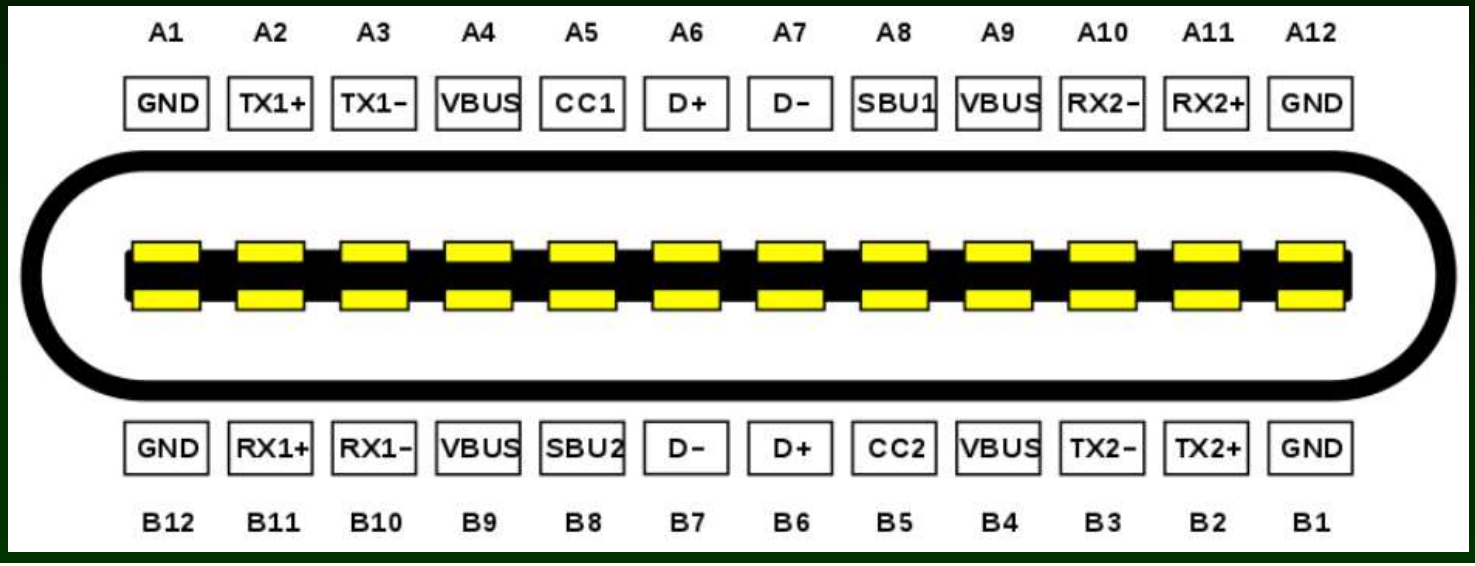
https://en.wikipedia.org/wiki/USB_3.0

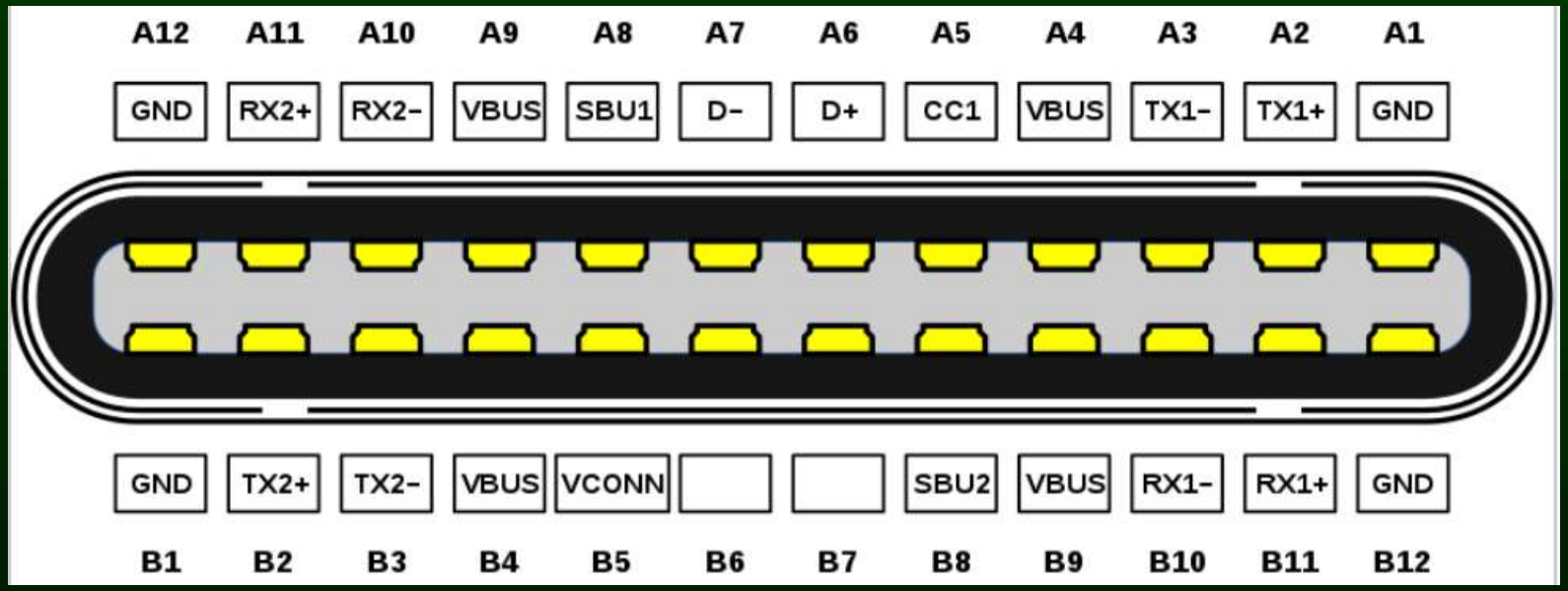
USB versions : USB C

Type-C receptacle A pin layout			Type-C receptacle B pin layout		
Pin	**Name**	**Description**	**Pin**	**Name**	**Description**
A1	GND	Ground return	**B12**	GND	Ground return
A2	SSTXp1	SuperSpeed differential pair #1, TX, positive	**B11**	SSRXp1	SuperSpeed differential pair #2, RX, positive
A3	SSTXn1	SuperSpeed differential pair #1, TX, negative	**B10**	SSRXn1	SuperSpeed differential pair #2, RX, negative
A4	V_{BUS}	Bus power	**B9**	V_{BUS}	Bus power
A5	CC1	Configuration channel	**B8**	SBU2	Sideband use (SBU)
A6	Dp1	USB 2.0 differential pair, position 1, positive	**B7**	Dn2	USB 2.0 differential pair, position 2, negative[a]
A7	Dn1	USB 2.0 differential pair, position 1, negative	**B6**	Dp2	USB 2.0 differential pair, position 2, positive[a]
A8	SBU1	Sideband use (SBU)	**B5**	CC2	Configuration channel
A9	V_{BUS}	Bus power	**B4**	V_{BUS}	Bus power
A10	SSRXn2	SuperSpeed differential pair #4, RX, negative	**B3**	SSTXn2	SuperSpeed differential pair #3, TX, negative
A11	SSRXp2	SuperSpeed differential pair #4, RX, positive	**B2**	SSTXp2	SuperSpeed differential pair #3, TX, positive
A12	GND	Ground return	**B1**	GND	Ground return

https://en.wikipedia.org/wiki/USB-C

USB versions : USB C





https://en.wikipedia.org/wiki/USB-C

Other famous buses: FireWire

- FireWire (IEEE 1394) (1995), i.Link
  - External serial bus of PCs (and isochronous devices).
  - Apple development. Sony: i.Link
- IEEE-1394a 2000.
- IEEE-1394b 2002.

- Fire Wire: 63 devices, hub
  - Multiple hosts (and no special chipset required for IP)
  - Devices can communicate without a CPU (peer-to-peer)
  - Plug-n-play support
  - Unregulated 25V (9 - 12V), 7 - 8 W load per port

FireWire versions

- FireWire 400
  - 100, 200, 400 Mbps speeds (in practice slightly lower: 98, 196, 392)
  - Cable length 4.5 m, but 16 devices can be chained together
    (daisy chain)
  - 6 or 4-pin connector, cable
- FireWire 800 (2003)
  - 786 Mbps, but compatible with 400 Mbps devices
  - 9-pin connector

Comparison

	Nyers sávszélesség (Mbit/s)	Átviteli sebesség (MB/s)	Max. kábel hossz. (m)	Áramot közvetít	Eszköz per csatorna
SAS	3000	300	8	Nem	4
eSATA	3000	300	2	Nem	1 (15 port sokszorosítóval)
SATA 3	6000	600	1	Nem	1 per vonal
SATA 2	3000	300	1	Nem	1 per vonal
SATA 1	1500	150	1	Nem	1 per vonal
PATA 133	1064	133	0,46	Nem	2
FireWire 800	786	98	4,5[1]	Igen (12–25 V, 15 W)	63
FireWire 400	393	49	4,5[1]	Igen (12–25 V, 15 W)	63
USB 2.0	480	≈ 40	5[2]	Igen (5 V, 2,5 W)	127
USB 3.0	4800	?	?	Igen (5 V, 2,5 W)	127
Ultra-320 SCSI (Ultra-4)	2560	320	12	Nem	16
Ultra-640 SCSI (Ultra-5)	5120	640	??	Nem	16
Fibre Channel rézkábelen	4000	400	12	Nem	126 (16777216 switch-csel)
Fibre Channel optikán	10520	2000	2–50 000	Nem	126 (16777216 switch-csel)

http://hu.wikipedia.org/wiki/Serial_ATA